Spectral PLL Built-In Self-Test for Integrated Cellular Transceivers

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***Abstract*— A built-in self test (BIST) solution for the on-chip spectral verification of a 4 GHz Phase-Locked Loop (PLL) is presented. The PLL is embedded in an integrated cellular RF transceiver in a 130 nm CMOS technology. The BIST blocks enable the detection of catastrophic and many parametric faults by measuring the PLL frequency response and checking for spurious sidebands and excessive in-band phase noise without external test equipment. Multi-tone stimuli with a spurious-free dynamic range (SFDR) of 60 dB are generated on-chip, the PLL RF response is demodulated and digitized in an on-chip digital FM discriminator. Spectral analysis is performed using digital narrowband filtering, achieving an SFDR of 45 dB. The fully digital BIST blocks require a chip area of only 0.06 mm^2 and do not compromise the performance of the PLL itself.**

I. Introduction

Until a few years ago, RF ICs were low complexity devices that required no Design-for-Test (DfT) or even BIST features for production test. Since then, a general trend towards wireless devices has turned RF ICs into high volume System-On-Chip (SOC) commodity products for consumer markets with dwindling gross margins. As a consequence, test costs account for a growing percentage of the total production costs, turning DfT and BIST into an economic necessity for RF ICs. However, area and yield limitations are extremely restrictive, favoring the use of compact, robust DSP solutions.

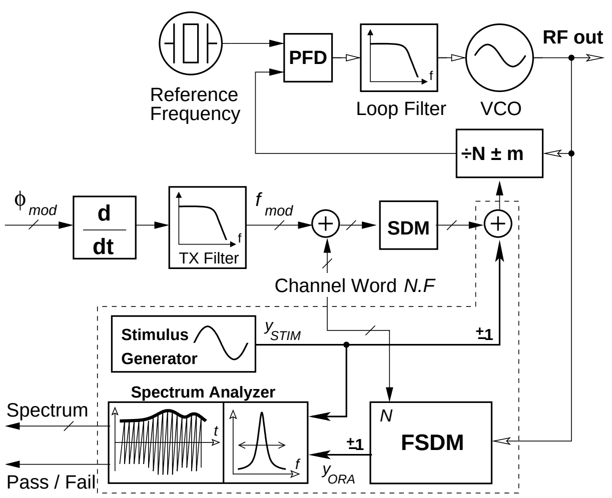


Fig. 1: ΣΔ–PLL with BIST blocks (dashed lines)

This paper presents a novel BIST approach for autonomous, specification oriented test of RF PLLs in SOCs which are especially hard to test because they are completely embedded. Spectral parameters like frequency response or the level of spurious sidebands have to be guaranteed for wireless applications. The focus of this paper is therefore compact on-chip spectral analysis without disturbing critical RF paths.

The BIST blocks have been integrated on an RF transmitter utilizing a sigma-delta modulated fractional–N PLL (Fig. 1). This architecture is commonly used for highly integrated RF CMOS transceivers because it is well adapted to CMOS technologies [1] and allows digital data modulation. The BIST functionality is achieved using robust, digital signal processing blocks with little area penalty due to the high integration density of the 130 nm CMOS technology.

Section II describes the generation of multi-tone test signals and the modulation of the PLL. Section III shows how to demodulate and digitize the RF signal without analog down-conversion or high-resolution ADCs. Section IV demonstrates an efficient way for on-chip spectral analysis of the demodulated bit stream by applying digital narrowband filtering and section V finally demonstrates first measurement results.

II. Stimulus Generation

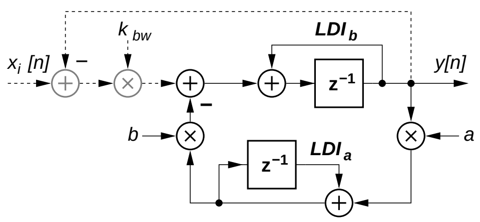


Fig. 2: LDI resonator

The digital stimulus generator has been realized with an undamped digital resonator made from lossless digital integrators (LDI) (Fig. 2, $k_{bw} = 0$). It has been shown that these structures are very robust against coefficient truncation while requiring minimum hardware [2]. The oscillation frequency ω_{ab} depends on the multiplication coefficients a and b and the sampling frequency f_S, amplitude $\hat{x}_a$ and phase ϕ_a are determined by the initial conditions $x_a[0]$. Multiple tones are generated by using time-division multiplexing. Further reduction of hardware complexity is achieved by replacing one multiplier with a fixed bit shifter ($a = 2^{-\alpha}$) and the other one by a sigma-delta attenuator.

This structure has been originally developed for the test of integrated ADCs [3] where also (1) – (3) have been derived. The approximations are valid for $x_b[0] = 0$ and small coefficients $|ab| \ll 1$:

$$\omega_{ab} = \arccos\left(1 - \frac{ab}{2}\right) f_S \approx \sqrt{ab}\, f_S \tag{1}$$

$$\phi_a \approx -\arctan\frac{2x_a[0]}{\sqrt{ab}} \approx \pi/2 \tag{2}$$

$$\hat{x}_a \approx \frac{x_a[0]}{\sin\phi_a} \approx x_a[0] \tag{3}$$

Besides saving area, the SDM attenuator has the additional advantage of providing a single bit stream that can be added easily to the oversampled divider sequence. Due to the inherent low-pass characteristic of the PLL (4th order, loop bandwidth 100 kHz) no filter is needed to remove the quantization noise from the bit stream.

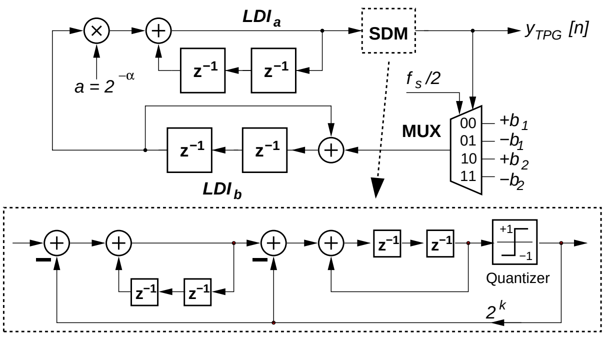


Fig. 3: Two-tone LDI oscillator using SDM attenuator

For this work, a two-tone generator has been implemented with a frequency range of $15\ldots180$ kHz running at a sampling frequency of 26 MHz. It achieves a spurious-free dynamic range of 60 dB with a word length of 15 bits and a coefficient length of 11 bits on a chip area of 0.025 mm^2.

The output frequency f_{out} of a fractional-N PLL with a reference frequency f_{ref} and a division ratio $N = N_I + N_F$, consisting of integer part N_I and fractional part $N_F = FRAC/2^{wf}$, is given by

$$f_{out} = f_{ref}\left(N_I + \frac{FRAC}{2^{wf}}\right) = N f_{ref} \tag{4}$$

where wf is the word length of the fractional accumulator and $FRAC$ is the fractional word. The PLL is frequency-modulated in the digital domain by adding modulation data $D[n]$ to the fractional word. The modulation data is low-pass filtered by the closed loop transfer function $G(s)$ of the PLL [4]. A fast

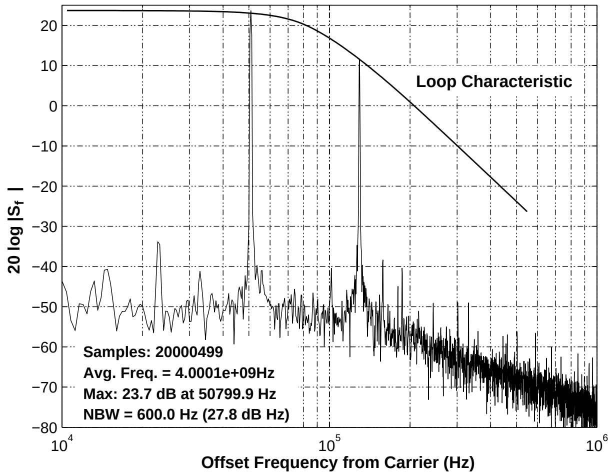


Fig. 4: Simulated two-tone spectrum at the PLL output

verification of $|G(s)|$ can be performed by using the two-tone generator from section II and measuring the frequency response. Within the loop bandwidth, $|G(s)| \approx 1$ and the digital data directly affects the PLL frequency (5).

$$f_{out}[n] \approx f_{ref}\left(N + \frac{D[n]}{2^{wf}}\right) \tag{5}$$

Higher modulation frequencies are attenuated by the loop characteristic: Fig. 4 shows the simulated FM–spectrum for a two-tone signal at the output of the PLL under test. The loop characteristic of the PLL is marked by the bold line. Simulations were performed with a standard VHDL simulator [5] including VCO and loop filter as VHDL models. Spectral information was obtained by post-processing the simulation data with Matlab.

III. Output Response Analysis

On-chip analysis of the modulated PLL signal requires demodulating and digitizing the RF signal which is a narrowband signal with rail-to-rail amplitude in the device-under-test. A standard down-conversion architecture requires large area, precision analog circuitry like a mixer and a high resolution ADC. Instead, a first order sigma-delta frequency modulator (SDFM) is used which only consists of a high-speed dual-modulus divider (DMD) and a D-flip-flop (Fig. 5) and delivers a sigma-delta modulated oversampled approximation of the frequency modulating signal.

This architecture has first been described in [6] to demodulate an FM signal at intermediate frequency. The high transit frequency of current CMOS technologies enables clocking the FSDM directly with the 4 GHz signal of the RF PLL to create an ultra-compact RF BIST architecture. The FSDM is realized with conventional flip-flops except for the RF stages where dynamic flip-flops are used, requiring only 0.0025 mm^2.

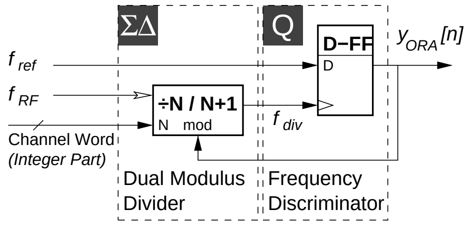


Fig. 5: First order sigma-delta frequency modulator

The DMD integrates the input frequency and subtracts N pulses depending on the MOD input. The D-FF acts as a coarse quantizer that compares the phase of the MMD to the reference phase and controls the DMD division ratio in such a way that the MMD output phase brackets the reference phase. Analog to conventional Sigma-Delta modulators, the first order FSDM has weak noise-shaping and strong spurious tones for certain input values. However, higher order FSDM as proposed in [6] require precision analog circuitry for RF applications which is incompatible to a robust BIST approach. Instead, section V shows a simple way to ameliorate these drawbacks.

IV. Spectral Analysis

Instead of implementing a full-blown FFT, a narrowband frequency analysis is performed to estimate the amplitude of frequency components (Fig. 7). First, the FSDM output bit stream with the sampling rate $f_S = 26$ MHz is decimated in a second order CIC filter by a factor of $R = 32$. Its magnitude transfer function is given by (6) [7].

$$|H(F)| = \left| \frac{\sin \pi F}{\sin \frac{\pi F}{R}} \right|^N \approx R^N \left| \mathrm{sinc} \pi F \right|^N \text{ for } F \ll 1$$
$$\text{with } F \doteq \frac{fR}{f_S} \tag{6}$$

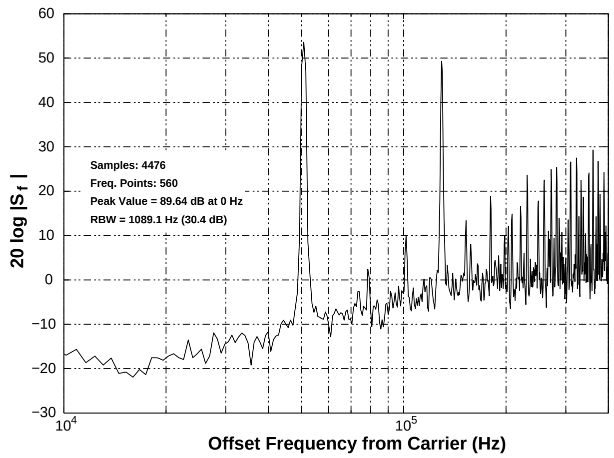


Fig. 6: Output spectrum of second order CIC decimator

Putting the passband edge at $F = 0.25$ (203 kHz) results in a magnitude response droop of 2 dB that can be corrected later on. However, the dominant aliasing components at $F = 2 - 0.25$ (1.42 MHz) is attenuated by only 36 dB (third order: 53 dB). Area limitations prevented using a higher order CIC filter with improved attenuation. As the quantization noise of the FSDM is still so far down at that frequency that the spectrum in Fig. 6 is achieved at the output of the CIC.

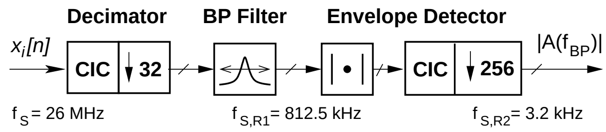


Fig. 7: Block diagram of amplitude estimator

The band of interest is selected with a narrow, programmable bandpass. It is implemented with a digital resonator (Fig. 2) as used in the multitone generator from section II. Here, the damping factor $k_{BW} > 0$ determines the bandwidth, it is implemented as a fixed bit-shift. A main advantage of this filter type is is its robustness against coefficient truncation: $a = b = k_f$ set the center frequency f_c with only 9 bits wordlength which gives a frequency resolution of 300 Hz without compromising noise performance or stability. Another advantage is that the resonance frequency f_c is set with a single parameter k_f (7).

$$f_c = \frac{f_{S,R1}}{\pi} \arcsin \frac{k_f}{2} \approx \frac{k_f f_{S,R1}}{2\pi} \tag{7}$$

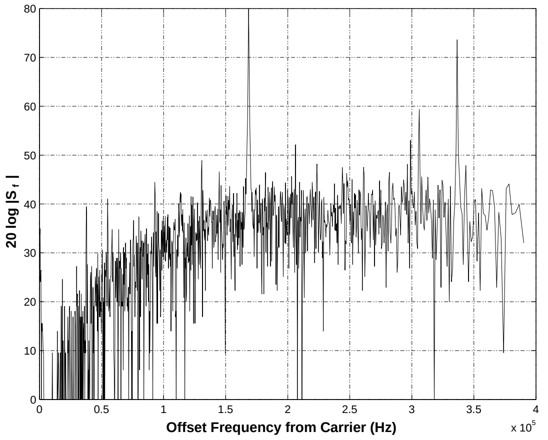
The reduced sampling rate of $f_{S,R1} = 812.5$ kHz enables resource sharing, here, a fourth order staggered band-pass with tunable center frequency is implemented with only one multiplier. Simultaneous multitone analysis could be performed at the cost of additional chip area by running several resonators in parallel [2].

The filter output is rectified and averaged in another CIC filter. The complete filter chain requires an area of 0.03 mm^2, the settling time is approx. 3 ms. The result is transferred asynchronously via a serial bus to the production tester or a PC, where some post-processing is performed like compensating the CIC characteristic and the non-linear frequency axes of test-tone generator and bandpass filter.

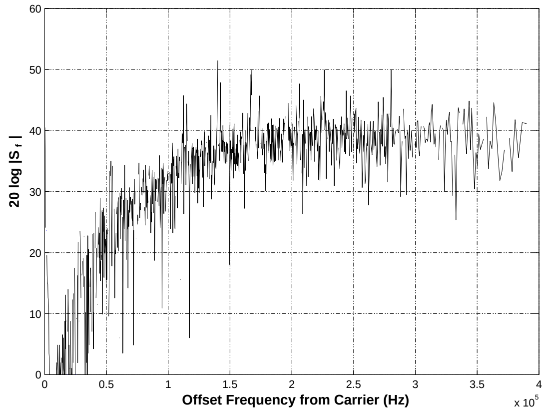
V. Measurements

The measurement plots in this section demonstrate the performance of the spectral BIST although only some critical frequency points would be measured under production test conditions to save test time.

A SFDR of 60 dB of the stimulus generator and a dynamic range of 90 dB of the filter chain was measured by directly connecting both blocks (Fig. 1). Feeding the FSDM with an unmodulated PLL signal produced the expected spurious tones (Fig. 8(a)).



(a)



(b)

Fig. 8: Unmodulated spectrum measured on-chip without (a) and with (b) selective averaging

As these tones are deterministic, their magnitude can be reduced by approximately 30 dB by averaging multiple measurements at PLL frequencies stepped by e.g. 10 kHz and selecting only data points that differ less than 10 dB between measurements (Fig. 8(b)). This procedure is feasible as the PLL takes only a few μs to lock to the new frequency.

Fig. 9 shows a two-tone spectrum measured on-chip with too weak attenuation of the out-of-band tone, indicating a faulty loop transfer characteristic. The two-tone modulation helps to distribute the spectral power of the spurious tones over the spectrum, achieving a SFDR of approx. 45 dB.

VI. Conclusions

An area efficient method for a spectral BIST of RF PLLs embedded in integrated RF transceivers has been presented. Multitone stimulus generation, modulation and demodulation of the PLL and spectral analysis rely entirely on digital components and have been implemented in a 130 nm CMOS technology in an area of only 0.06 mm^2. Both stimulus generator and tunable narrowband filter are based on digital resonators that allow the use of short coefficients without

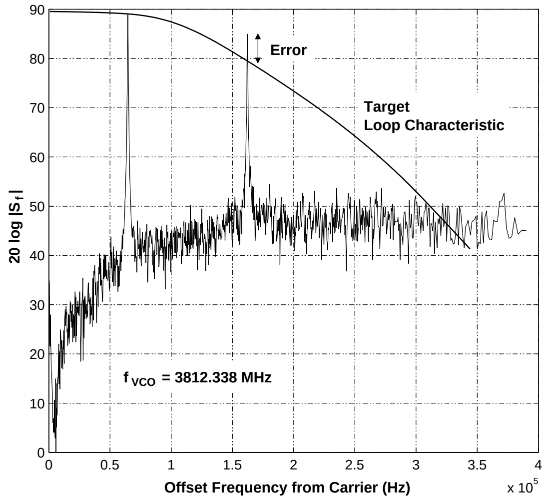


Fig. 9: Two-tone PLL spectrum measured on-chip

performance degradation. The coefficients are directly related to the target parameters center frequency and bandwidth, enabling single coefficient tuning.

Overall SFDR is approximately 45 dB, mainly limited by the spurious tones of the first order FSDM. Although performance could be improved at the cost of additional analog circuitry and more complex digital signal processing, the presented minimum area solution improves test coverage for embedded PLLs to a degree that will be sufficient for many applications.

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