



DATE '07, April 16-20, 2007, Nice, France

RF Built-In Self-Test (BIST) for Integrated Cellular Transmitters

BIST Requirements

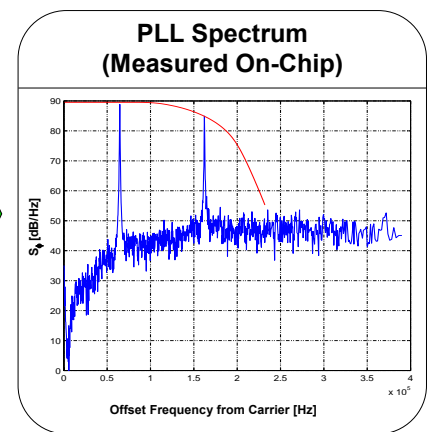
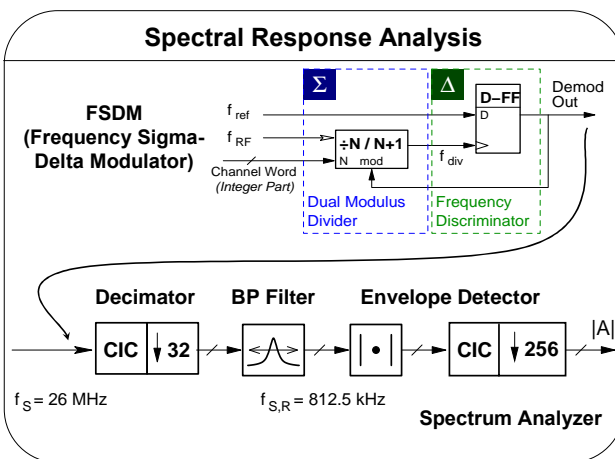
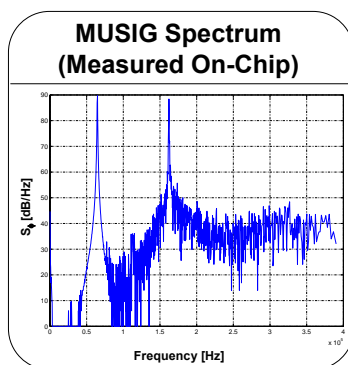
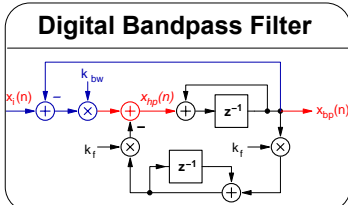
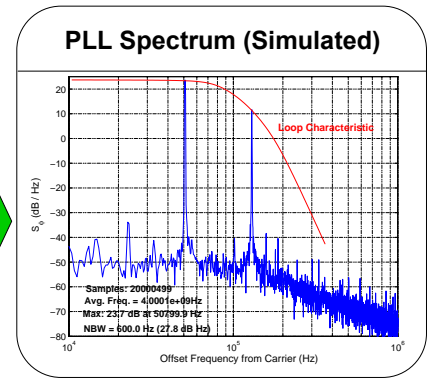
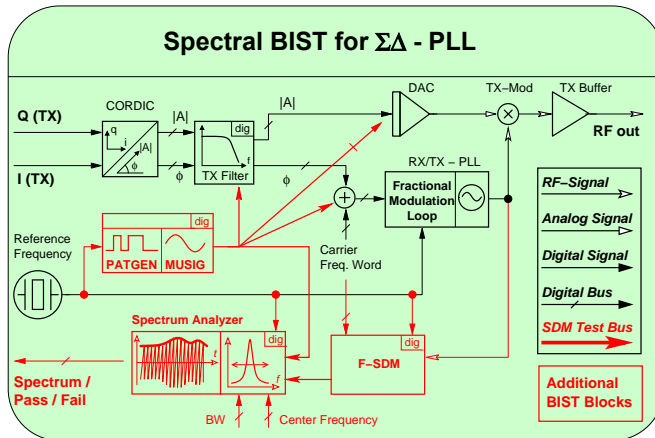
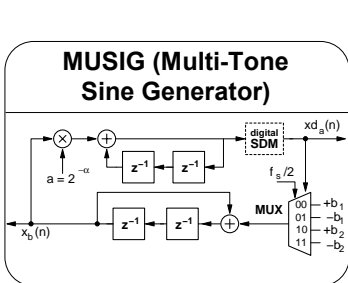
- Small silicon area
- Fully digital implementation
- No interference with critical RF paths
- Spectral analysis of PLL performance

BIST Concept

- Digital multitone generator provides PLL test stimuli
- Digital FM discriminator demodulates PLL RF signal
- Digital narrowband filter and envelope detector analyze spectral response

BIST Implementation

- Implemented for a 4 GHz $\Sigma\Delta$ - PLL
- Area: 0.05mm² in 130nm CMOS
- 2 programmable tones with a frequency between 30 ... 300 kHz
- 4th order BP filter tunable in 300 Hz steps
- First measurement results prove feasibility



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