

# A transformer based 1.8-GHz low-IF receiver for 1V in 0.13- $\mu$ m CMOS

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## Introduction

A fully integrated low-IF receiver for 1.8GHz in 0.13- $\mu$ m CMOS is presented. The receiver consists of a VCO, an IQ-divider, an LNA, and a double balanced IQ-mixer. The RF input stage and the commutating stage of the IQ-mixer are current coupled via an on-chip transformer which is operating in resonant mode and is performing a current gain. A design method is presented to reduce the input impedance of the mixer's commutating stage in order to improve the current gain of the on-chip transformer. The receiver takes 25.7mA from a 1-V supply to give an input IP3 of -20.3dBm, an input referred 1-dB compression point of -30.7dBm, a conversion gain of 29.2dB and a noise figure of 3.0dB.

## LNA and Mixer

Fig. 1 shows a block diagram and all subcircuits (except the mixer) of the proposed receiver. For the differential LNA a LC-tank load has been used to avoid a DC voltage drop at the output. The AC coupled feedback resistors put the input impedance of the LNA into a region where the 200- $\Omega$  input matching can easily be done with one external inductor and two external capacitors.

The mixer employs an on-chip transformer to establish a current coupling between the RF input stage and the commutating stage. Although the on-chip transformer is known as a lossy element it can achieve a high current gain if it is operating in resonant mode and the differential output resistance of the RF input stage of the mixer is high and the differential input resistance of the commutating stage is as low as possible. The current gain of the on-chip transformer helps to improve the IP3 and to reduce the power consumption of the mixer [1], [2].

A high output resistance of the RF input stage is achieved by the use of the cascode transistors  $N_3$  and  $N_4$  (Fig. 2). In previously published transformer based mixers [1] – [5] the commutating stage is directly connected to the secondary winding of the transformer, and therefore the transistors of the commutating stage must have a high transconductance to

decrease their differential input resistance. A high transconductance requires wide devices or a high drain current, which loads the local oscillator or increases the power consumption and the DC voltage drop across the output resistors respectively.

In the mixer of this work (Fig. 2) the transistors  $N_5 - N_8$  are connected between the secondary winding and the commutating stage.  $N_5 - N_8$  can be made wide without deteriorating the frequency behavior of the on-chip transformer since a capacitance in vicinity of some picofarad needs to be connected to the secondary winding anyway to put the on-chip transformer into resonant mode. Because of the great width of  $N_5 - N_8$  the input resistance of the commutating stage is reduced while the drain current of  $N_5 - N_{16}$  and the width of  $N_9 - N_{16}$  can be small.  $N_5 - N_8$  helps also to isolate the RF input signal from the LO signal to suppress self mixing. With the potential at the gates of  $N_5 - N_8$  the output common mode level of the mixer can be set up.

## Local Oscillator

The VCO uses an NMOS and a PMOS cross coupled pair without a constant tail current source. This ensures that the output voltage swings between the supply rails, contrary to a design with only NMOS or PMOS transistors and a differential coil connected with its center tap to either the positive or negative supply rail respectively, so the output voltage swing would roughly be twice the supply voltage, decreasing the phase noise but also decreasing the life time of the VCO because of severe MOS degradation (hot electron effects) or even gate oxide breakdown. Due to the current reuse in the structure with both NMOS and PMOS devices nearly half the power consumption is necessary for the same negative resistance. The current source under the NMOS cross coupled pair (or over the PMOS cross coupled pair respectively) is omitted to maximize the output voltage swing and to lower flicker noise terms and therefore to reduce the phase noise [6], [7]. To cope with the low supply voltage of 1V the constant tail current sources of the D-flipflops have also been omitted.

## Experimental Results

An external 1:4 balun has been used to perform the impedance transformation from the single ended 50- $\Omega$  signal generator to the differential 200- $\Omega$  input of the LNA, therefore all simulation and measurement results refer to a 50- $\Omega$  source. Fig. 3 shows the gain and the input return loss over the RF input frequency for a constant intermediate (IM) frequency by sweeping the RF input frequency and the local oscillator (LO) frequency at the same time. Fig. 4 shows the IP3 curves for RF input frequencies of 1.8GHz and 1.801GHz and a LO

frequency of 1.79GHz. The table in Fig. 5 summarizes and compares the simulation and measurement results. Fig. 6 shows a photograph of the die.

## Layout

The chip has been realized in Infineon 0.13- $\mu\text{m}$  standard low cost CMOS process with six metal layers. The die consumes an area of 1.8mm x 1.2mm. Differential coils have been used for the LNA, the VCO, and the on-chip transformer. Therefore the inductance per area is increased because of the magnetic coupling between the interleaved wound coils, and the parasitic capacitance at the center tap cancels out because of the balanced configuration. For this reason the center tap is at the outermost winding and these windings are wider than the inner ones to reduce ohmic losses. The upper three metal layers were used in parallel and were merged with via bars to lower the ohmic losses. A detailed discussion of the design of an on-chip transformer to achieve a high current gain is given in [1] and [2].

## References

- [1] C. Hermann, M. Tiebout, H. Klar, "A 0.6V 1.6mW Transformer based 2.5GHz Downconversion Mixer with +5.4dB Gain and -2.8dBm IIP3 in 0.13 $\mu\text{m}$  CMOS" in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, pp. 35-38, 2004, 6-8 June 2004.
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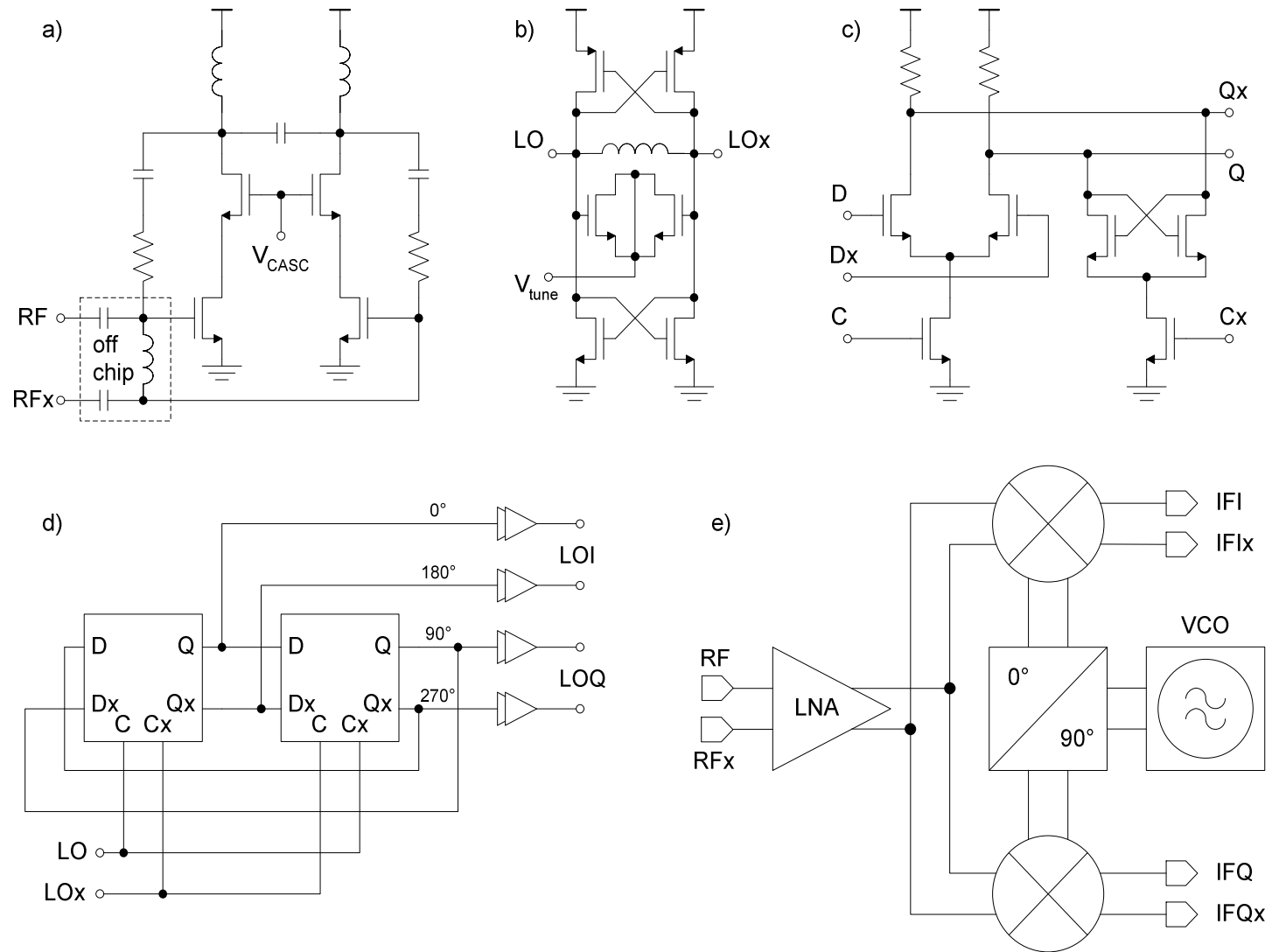


Fig. 1. a) LNA (biasing not shown), b) VCO, c) D-flipflop, d) IQ-Divider, e) Block diagram of the receiver

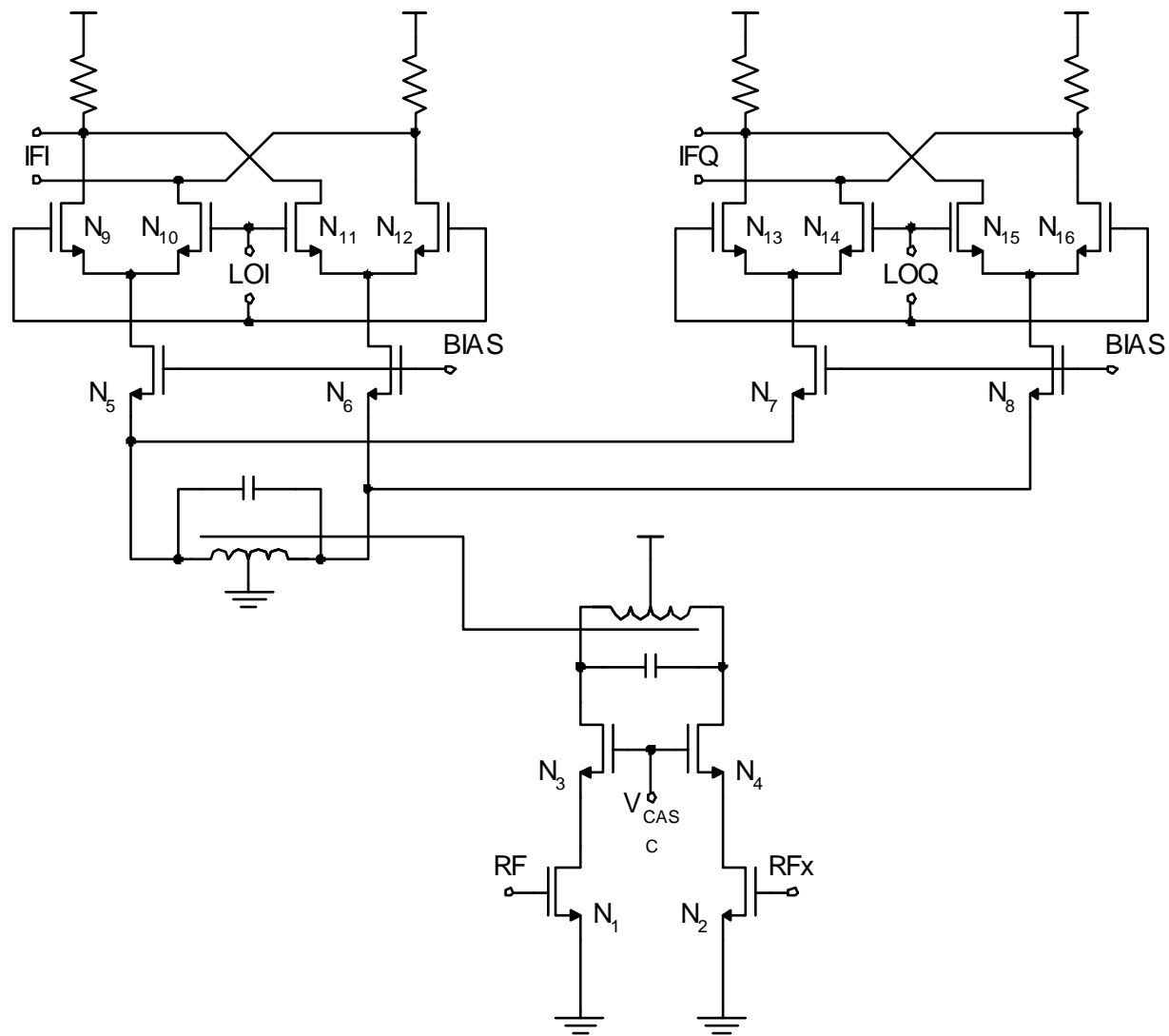


Fig. 2. IQ-mixer of the proposed receiver.  $N_5 - N_8$  reduce the input resistance of the commuting stage to improve the current gain of the on-chip transformer.

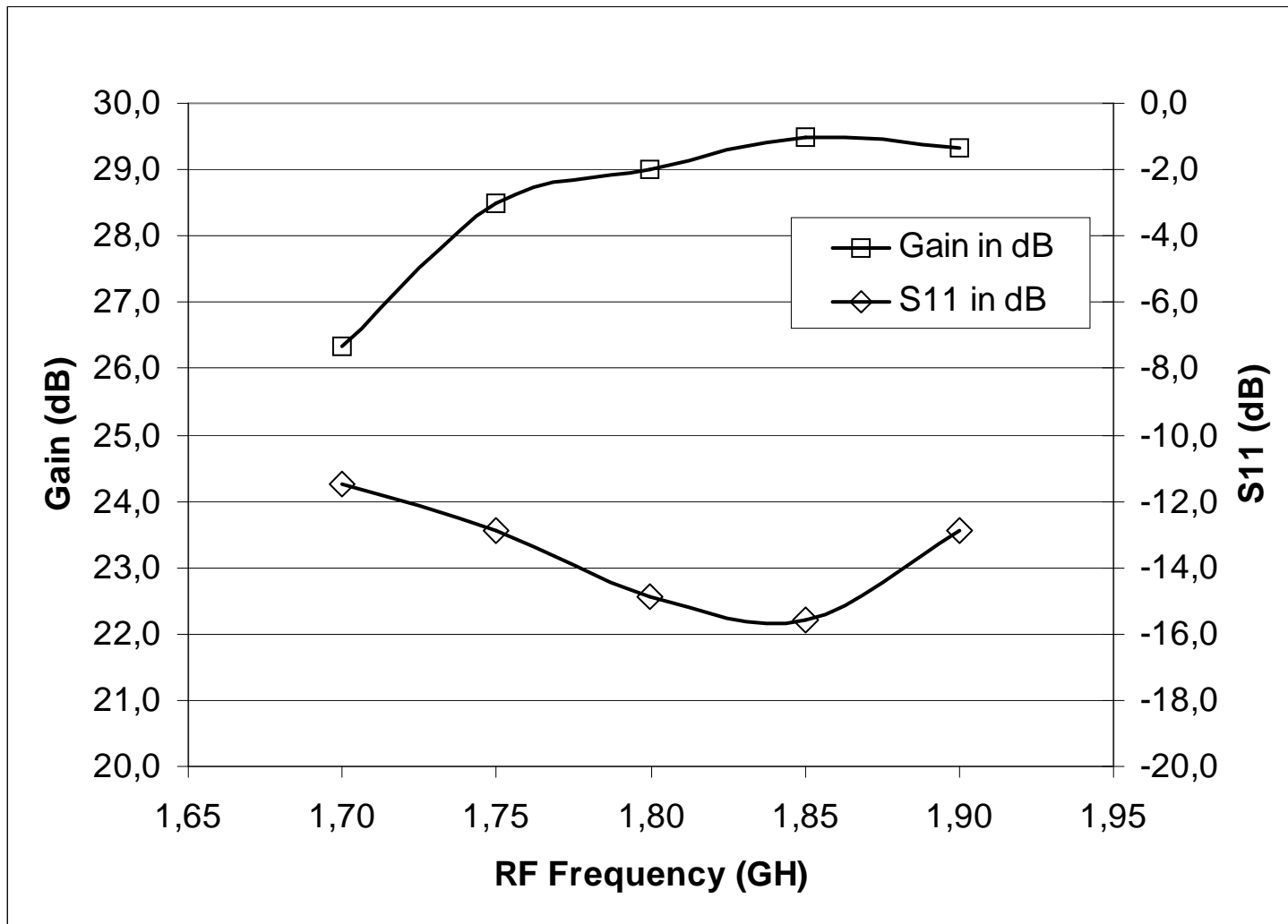


Fig. 3. Gain and  $S_{11}$  over RF frequency. The gain is 29.5dB at the center frequency of 1.85GHz. The input return loss is <11.5dB in the frequency range of 1.7 – 1.9GHz.

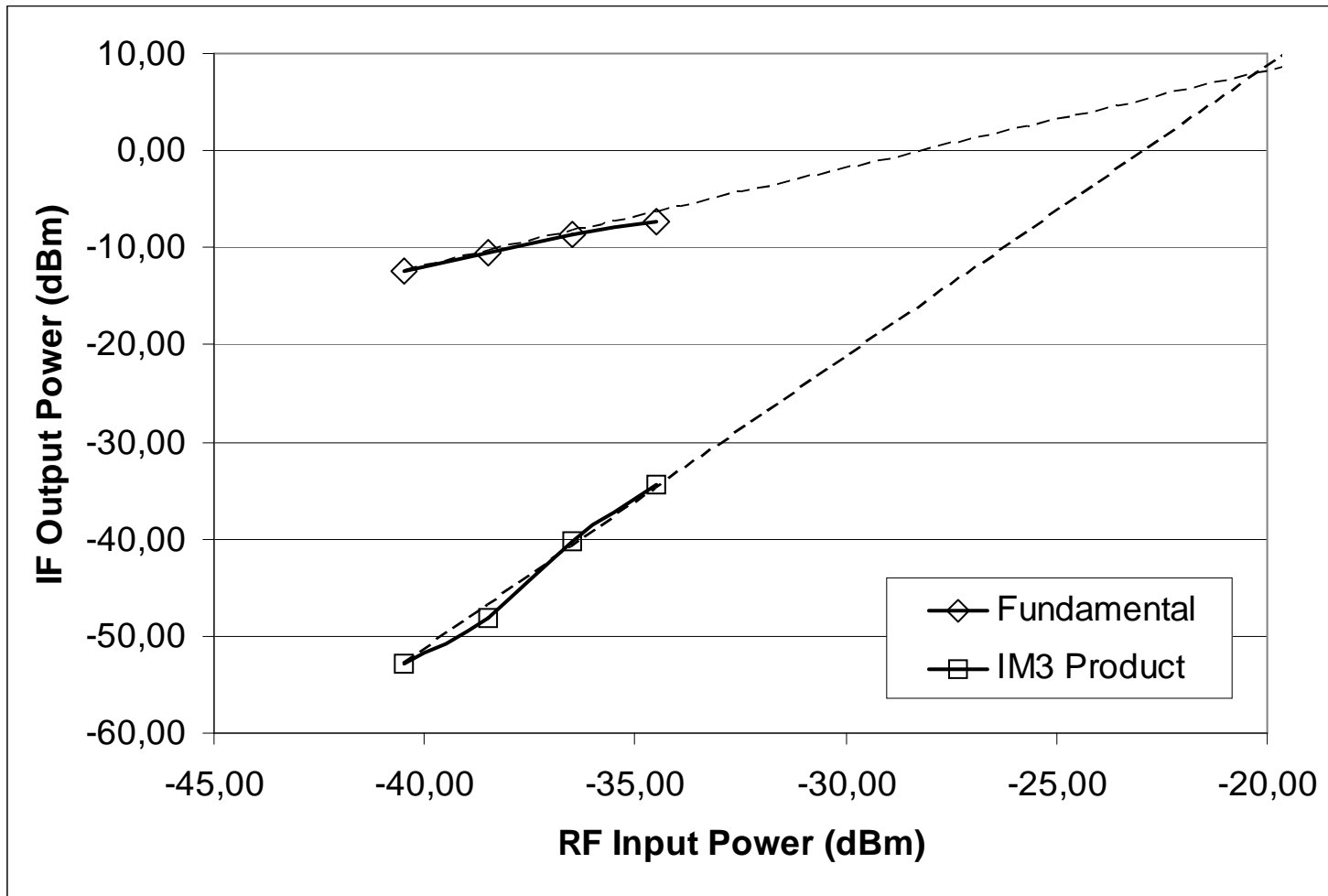


Fig. 4. IP3 curves. The input IP3 is -20.3dBm. The RF input frequencies have been set to 1.8GHz and 1.80005GHz. The LO frequency has been set to 1.799GHz.

Supply Voltage (V)	1.0
Current Consumption (mA)	25.7
Power Consumption (mW)	25.7
Gain (dB)	29.2
Noise Figure (dB)	3.0
Input Return Loss @ 1.8GHz (dB)	-14.9
Input referred 1-dB-Compression (dBm)	-30.7
Input IP3 (dBm)	-20.3
VCO Tuning Range (GHz)	3.4 - 3.8
Nominal RF input Frequency (GHz)	1.8
RF-IF Isolation (dB)	-55.0
LO-IF Isolation (dB)	-51.5
Technology	0.13- $\mu$ m CMOS
Chip Area (mm <sup>2</sup> )	2.16

Fig. 5. Experimental results.

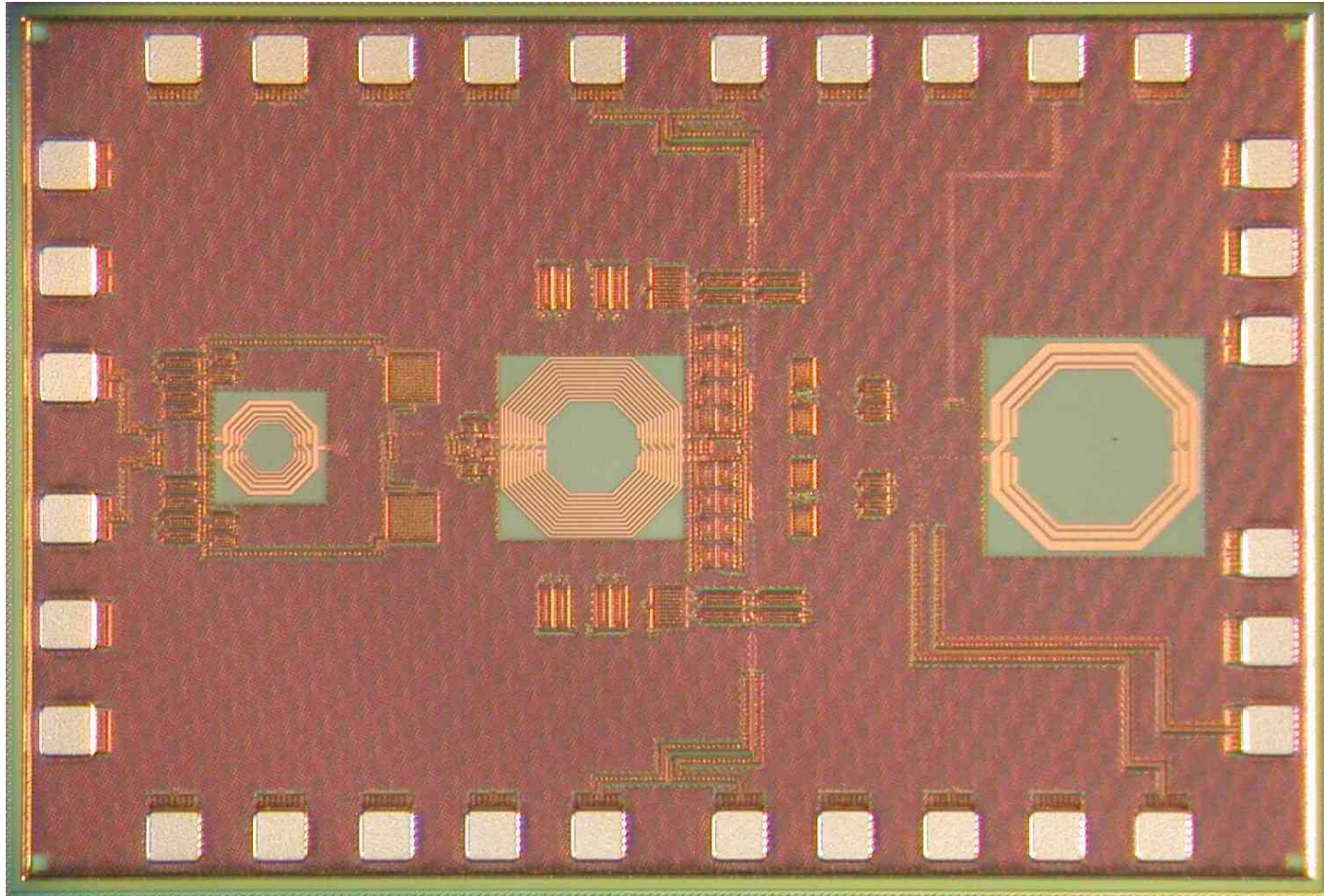


Fig. 6. Die Photo.