

RF Built-In Self-Test for Integrated Transmitters Using Sigma-Delta Techniques

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Abstract—A new approach to adding built-in self test (BIST) capabilities to integrated sigma-delta modulation RF transmitters is presented. An area efficient, all-digital building block generates multitone FM stimulus signals without compromising the performance of the RF transmitter itself. The RF signal is demodulated and digitized in a on-chip digital FM discriminator. Both blocks are fully testable using standard scan chain methods and consume a chip area of only 0.03 mm^2 in a 130 nm CMOS technology. The spectral quality and reproducibility of the test signals are suitable for intermodulation distortion tests or PLL frequency response measurements.

I. INTRODUCTION

In the 1980's digital ICs had reached a complexity level that caused poor test coverage in spite of exploding production test times. As a consequence, design-for-test (DfT) methodologies like scan chains, boundary scan and built-in self test (BIST) became an integral part of digital IC design flow. During the 1990's similar concepts were implemented on mixed-signal ICs, mainly to speed up the time consuming production tests of high-resolution ADCs and DACs [1]–[3].

Until a few years ago, production test for RF ICs required a good understanding of RF measurement techniques but little DfT support. RF ICs were low-complexity devices manufactured in special high-performance technologies, surrounded by a plethora of passive and active components on the PCB. Now, even mainstream CMOS technologies have transit frequencies exceeding 100 GHz, enabling e.g. the integration of RF transceiver and base-band processor on one chip. Fired up by a general trend towards wireless devices, RF ICs have become highly integrated, high volume commodity products for consumer markets with fierce competition and shrinking profit margins.

As a consequence, test costs account for a growing percentage of the total production costs. Once more, testability and production test have become a bottle-neck for IC manufacturers, turning DfT and BIST into an economic necessity for RF ICs as well.

Modern CMOS processes facilitate enormous integration densities but due to their large statistical parameter spread and low supply voltages they are not optimized for analog or

RF performance. This makes not only the design of analog and RF circuitry a challenging task, there is also an increased risk of parametric failures in the analog BIST circuitry itself. Interfering with critical RF paths on chip is also undesirable due to possible performance degradation. On the other hand, the high integration density of deep submicron CMOS technologies allows the realization of complex digital signal processing blocks with little area penalty. This favors the digital implementation of on-chip test circuitry: it is compact and robust and it can be tested using well established digital test methodologies.

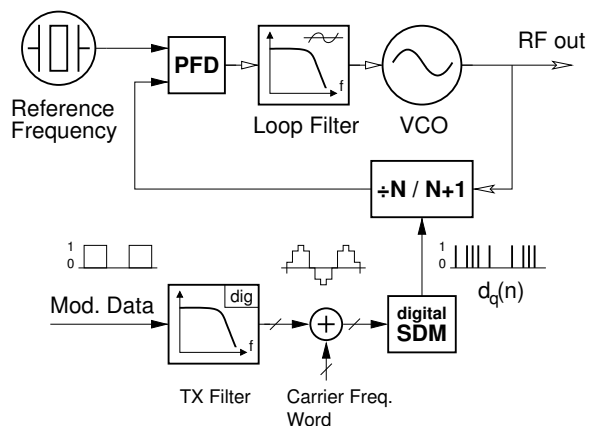


Fig. 1. Digital $\Sigma\Delta$ modulation transmitter

This paper presents a fully digital BIST concept for wireless RF transmitters that allows testing key parameters without disturbing performance critical analog paths. Catastrophic and also some parametric failures can be identified quickly. The focus of this paper is on transmitter architectures utilizing a digital sigma-delta modulator (fig. 1). This architecture is commonly used for highly integrated RF CMOS transceivers because it is well adapted to CMOS technologies [4].

Section II gives an overview over the proposed test concept, section III describes the generation of digital multitone stimuli and section IV the upconversion of these stimuli to the RF domain. Section V shows a solution for demodulating and

digitizing the RF signal in a compact digital building block. Section VI demonstrates how the concepts were integrated on a GSM transceiver test chip.

II. TEST CONCEPT

Recently, several loop back test concepts have been proposed for integrated RF transceivers where the on-chip receiver (RX) demodulates the RF signal generated by the transmitter (TX) [5], [6]. While loop back concepts look very appealing due to low area overhead and high test coverage, there are some pitfalls for the practical implementation: Most chips built for time-division multiplex access systems like GSM or Bluetooth are not specified (and often not capable) of running the RX and TX path at the same time. Often, both paths share the local oscillator (LO) to save chip area. Even when RX and TX do have independent LO generation, there is a high risk of injection lock-in between two oscillators running at nearly the same frequency. Besides, most standards use frequency division duplexing which means either RX or TX path would have to operate outside its specified frequency range during a loop back test.

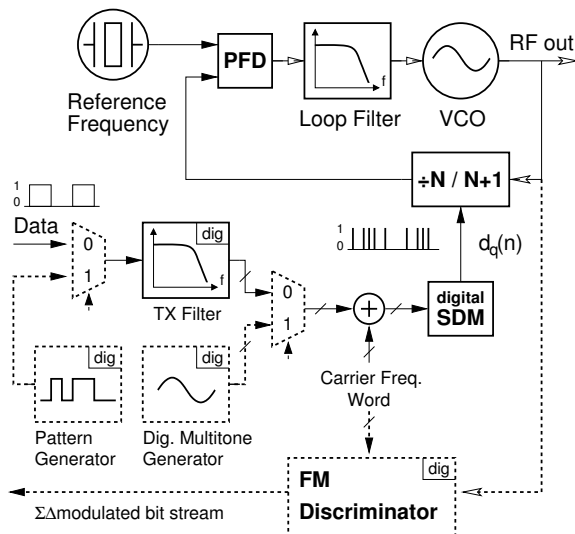


Fig. 2. Fractional- N modulator with added BIST blocks

On-chip analysis of the transmit signal requires extracting and digitizing the RF phase / frequency information from the carrier. Standard receiver architectures apply analog downconversion and high-resolution ADCs. They are optimized for receiving low-level RF signals in the presence of strong interferers and require large area, precision RF analog circuitry which makes them unsuitable for implementation as additional BIST circuitry.

As the transmitter provides a narrowband signal with large, constant amplitude, a much simpler demodulation technique can be applied: a first order digital FM discriminator consists of simple, compact digital blocks and delivers a sigma-delta modulated bit stream that can be further analyzed in the

digital domain on- or off-chip.

A suitable stimulus signal for the transmitter is generated by a digital multi-tone sine generator and upconverted to RF by the sigma-delta modulation transmitter (Fig. 2) that acts as a sort of DAC converting digital data into RF phase/frequency [7].

Multitone FM signals can e.g. be used to measure intermodulation distortion or the frequency response of the PLL: the amplitude of a sideband within the passband is compared with another one outside the passband to check whether the closed loop bandwidth of the PLL is within the specified limits (Fig. 8).

This fully digital stimulus generation and RF analysis does not interfere with the critical RF paths.

III. DIGITAL MULTI-TONE GENERATION

Multitone tests have been used for a long time to characterize intermodulation distortions and frequency response of amplifiers, ADCs or RF modulators / demodulators. [3] presents a mixed A-D built-in self test (MADBIST) scheme consisting of digital biquad oscillators and a $\Sigma\Delta$ DAC for generation of multi-tone test signals to test both baseband ADCs and DACs. [8] extends this approach into the RF domain by using higher order images of a digital test signal to verify an RF receiver. Disadvantages of this method are that the amplitude of the higher order images is not very predictable and that two multiplexers need to be inserted into the critical RF path.

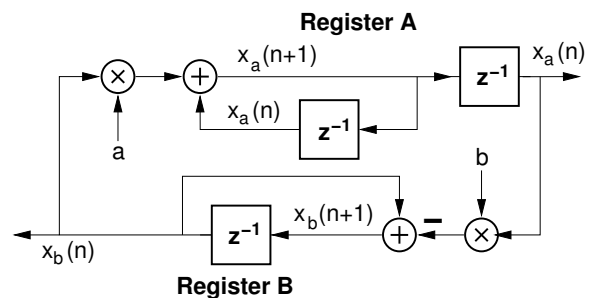


Fig. 3. Digital biquad oscillator

The main building block for generating multi-tone signals in [3] is a digital biquad oscillator with quadrature outputs $x_a(n)$, $x_b(n)$ (fig. 3), realized with lossless digital integrators (LDI).

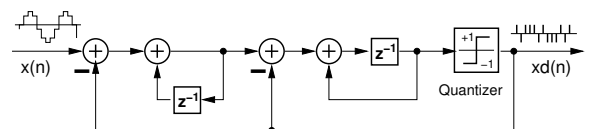


Fig. 4. Second order sigma-delta modulator

Relations for output signal frequency ω_{sig} , amplitude x_a, x_b and initial phase ϕ_a, ϕ_b of the biquad depending on sampling frequency f_s , coefficients a, b and the initial conditions $x_a(0), x_b(0)$ are derived in [9]:

$$\omega_{sig} = f_s \cos^{-1} \left(1 - \frac{ab}{2} \right) \quad \text{for } 0 < ab \leq 2 \quad (1)$$

$$\phi_a = \tan^{-1} \frac{\sin(\omega_{sig} T_s) x_a(0)}{(1 - \cos(\omega_{sig} T_s) x_a(0) - ab) + ax_b(0)} \quad (2)$$

$$\hat{x}_a = \frac{(1 - ab) x_a(0) + ax_b(0)}{\sin(\omega_{sig} T_s + \phi_a)} \quad (3)$$

Results for ϕ_b and \hat{x}_b are attained by exchanging x_a with x_b and a with $-b$. For small coefficients $|ab| \ll 1$, the following approximations hold true:

$$1 - \cos \sqrt{ab} \approx \frac{ab}{2} \quad \text{and} \quad \cos^{-1} \left(1 - \frac{ab}{2} \right) \approx \sqrt{|ab|}$$

Using these approximations and setting $x_b(0) = 0$ gives the simplified relations

$$\omega_{sig} \approx \sqrt{ab} f_s \quad (4)$$

$$\phi_a \approx -\tan^{-1} \frac{2x_a(0)}{\sqrt{ab}} \approx \pi/2, \quad \phi_b = 0 \quad (5)$$

$$\hat{x}_a \approx \frac{x_a(0)}{\sin \phi_a} \approx x_a(0), \quad \hat{x}_b \approx x_a(0) \sqrt{\frac{b}{a}} \quad (6)$$

showing that amplitude, frequency and phase for the test tone can be set independently. The initial conditions can be optimized ($x_b(0) \neq 0$) for equal amplitudes x_a and x_b if precise quadrature signals are needed.

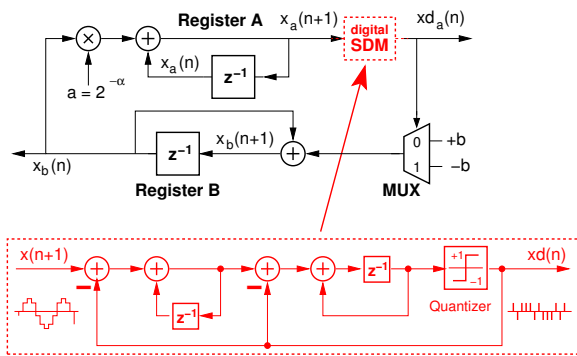


Fig. 5. Digital biquad oscillator using SDM attenuator

Directly implementing the circuit of fig. 3 in hardware would require two large area $N \times N$ bit multipliers. Another, more area efficient approach, is achieved by replacing one multiplier with a bit shifter, restricting the coefficient a to values of the form $2^{-\alpha}$. The second multiplier is implemented with a *sigma-delta attenuator* to achieve a fine granularity for the output frequency with only moderate area requirements

[3]: A sigma-delta modulator (SDM) (fig. 4) converts an N -bit wide stream $x(n)$ into an oversampled single-bit stream $xd(n)$. Multiplying the single-bit stream with a constant b now only requires an $N \times 1$ multiplier which is implemented as a multiplexer (fig. 5). In order to maintain the stability of the oscillator, an SDM like in fig. 4 with a latency of one sample clock has to be used. The sine signal is reconstructed from the oversampled data stream by simple low-pass filtering.

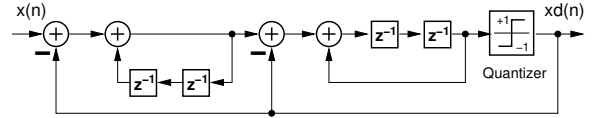


Fig. 6. Second order sigma-delta modulator for two time-multiplexed signals

Multitone signals can be generated by adding the signals of two or more sine generators. A more economic approach is achieved by sharing the oscillator hardware using time division multiplexing [3]. For each tone, registers have to be provided in the SDM (fig. 6) and the oscillator (fig. 7) so that the tone signals can be processed independently. The adders and the bit shifter are shared between the signals saving approx. 50% chip area compared to generating the tones individually.

Due to the time division multiplexing, the effective sampling frequency for L tones is reduced by a factor of L :

$$f_{s,eff} = f_s/L \quad (7)$$

This limits the useful number of tones, (8) gives a rule-of-thumb for the usable bandwidth of the oscillator [3].

$$f_{BW} \approx f_{s,eff}/150 \quad (8)$$

The achievable spurious free dynamic range (SFDR) of the multi-tone signal is difficult to calculate because the quantization error is not uncorrelated from the signal. Therefore, the signal spectrum will contain discrete sidebands reducing the SFDR. An SFDR of 60 dB was achieved in simulations with a word length of 15 bits.

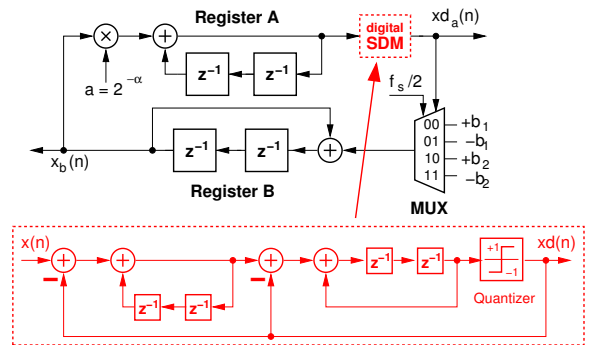


Fig. 7. Digital two-tone biquad oscillator using SDM attenuator

IV. RF SIGNAL GENERATION

Multi-tone FM / PM RF stimuli are easily generated by combining the multi-tone generator from the last section with a digital sigma-delta modulation transmitter. Due to the inherent low-pass characteristic of the PLL, no additional filter is needed to reconstruct the sine tones from the oversampled data stream of the test-generator.

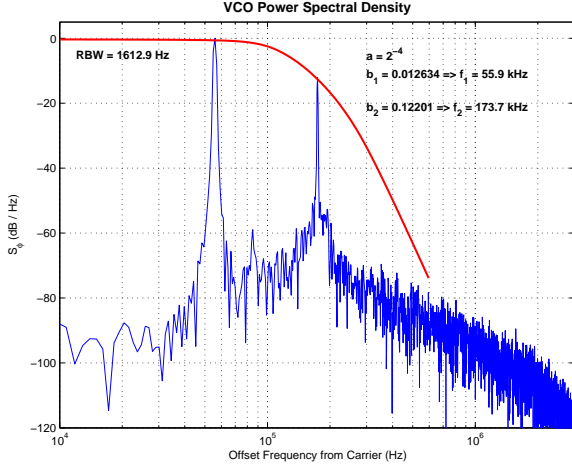


Fig. 8. Simulated two-tone spectrum at the PLL output

The output frequency f_{out} of a fractional-N PLL with a reference frequency f_{ref} and a division ratio N , consisting of integer part N_I and fractional part $N_F = FRAC/2^{wf}$, is given by

$$f_{out} = f_{ref} \left(N_I + \frac{FRAC}{2^{wf}} \right) = f_{ref} \cdot N_I \cdot N_F = f_{ref} \cdot N \quad (9)$$

where wf is the word length of the fractional accumulator and $FRAC$ is the fractional word. With such an architecture phase / frequency modulation of the PLL can be achieved by adding digital modulation data $D(n)$ to the fractional word:

$$N(n) = N_I + \frac{FRAC + D(n)}{2^{wf}} \quad (10)$$

The digital modulation of the division ratio is filtered by the closed loop transfer function $G(s)$ of the PLL (fig. 9) [10]:

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{N(s)}{1 + \frac{N}{K_P K_{VCO}} \frac{s}{Z(s)}} = N(s)G(s) \quad (11)$$

$N(s)$ is the representation of $N(n)$ in the complex frequency domain. Within the loop bandwidth, $G(s)$ is approximately unity and the digital data directly affects the PLL frequency:

$$f_{out}(n) \approx f_{ref} \left(N_I + \frac{FRAC + D(n)}{2^{wf}} \right) \quad (12)$$

When $D(n)$ is a digital sinewave with frequency f_{mod} and amplitude $\hat{m} = \max[D(n)] = 2^{w_{mod}}$, a peak PLL frequency deviation is created of

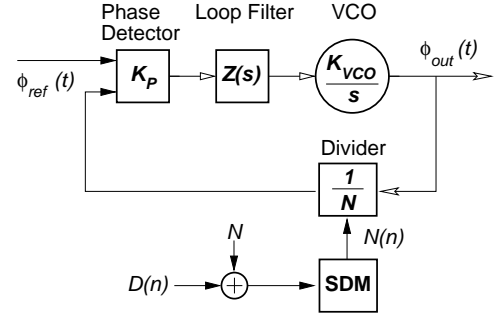


Fig. 9. Principle of fractional-N modulator

$$\hat{\Delta}f = 2^{w_{mod}} / 2^{wf} f_{ref} = 2^{w_{mod}-wf} f_{ref}, \quad (13)$$

where $w_{mod} < wf$ is the word length of the modulation word. This corresponds to a peak modulation index $\hat{\mu}$ of

$$\hat{\mu} = \hat{\Delta}f / f_{mod} = 2^{w_{mod}-wf} \frac{f_{ref}}{f_{mod}}. \quad (14)$$

V. DIGITAL FM DISCRIMINATOR

An digital FM discriminator and digitizer (Fig. 10) has first been proposed for demodulating an FM IF signal in 1994 [11]. At that time, multi-GHz dividers could only be implemented in ECL technology, requiring considerable chip area and power. Nowadays they can be realized as low-power, compact CMOS logic building blocks, enabling their use in RF BIST applications.

To avoid aliasing, the frequency deviation of the input signal has to be band-limited

$$f_1 < f_{ref}/2 \quad (15)$$

which is automatically fulfilled as the PLL bandwidth has to be much lower than f_{ref} due to stability reasons. Just as the input signal of a sigma-delta ADC must not exceed the quantizer input step $\pm q$ to avoid an overload condition, the input frequency f_{RF} of the sigma-delta frequency discriminator has to be within the limits

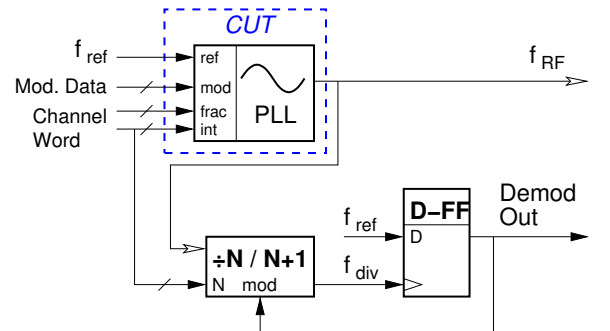


Fig. 10. First order FM discriminator with circuit-under-test (CUT)

$$Nf_{ref} < f_{RF} < (N+1)f_{ref}. \quad (16)$$

If these conditions are fulfilled, the demodulated output signal in fig. 10 is an oversampled, sigma-delta modulated approximation of the frequency modulating signal. Fig. 11 shows the simulation plot of a demodulated two-tone signal, achieving an SNR of nearly 90 dBc.

VI. IMPLEMENTATION

Functional and RF performance simulations were performed with a standard VHDL simulator, using the methodology described in [12], [13]: The complete circuit in fig. 2 including the analog blocks like VCO and loop filter was modeled in VHDL, the simulated period data of the VCO and the demodulated bit stream of the FM discriminator were dumped to a text file and post-processed using Matlab. Fig. 8 shows the simulated two-tone test signal at the output of a PLL with a loop bandwidth of 100 kHz, the x-axis being the offset frequency from the carrier. The low-pass characteristic of the PLL is marked by the bold line. One tone is outside the loop bandwidth, it is attenuated by approx. 12 dB compared to the in-band tone. This ratio can be easily verified in a production test setup using a spectral analyzer. The spurious free dynamic range is nearly 60dB which is more than sufficient for frequency response measurements.

Two different programmable test tone generators have been synthesized and put on a GSM transceiver test chip in a 130 nm CMOS technology. Table I shows the achieved frequency range and the chip area (excluding interconnect area).

Tones	Word Length	Min. Freq.	Max. Freq.	Area
1	15	31 kHz	365 kHz	0.01 mm ²
2	15	15 kHz	182 kHz	0.015 mm ²

TABLE I
IMPLEMENTED TEST-TONE GENERATORS

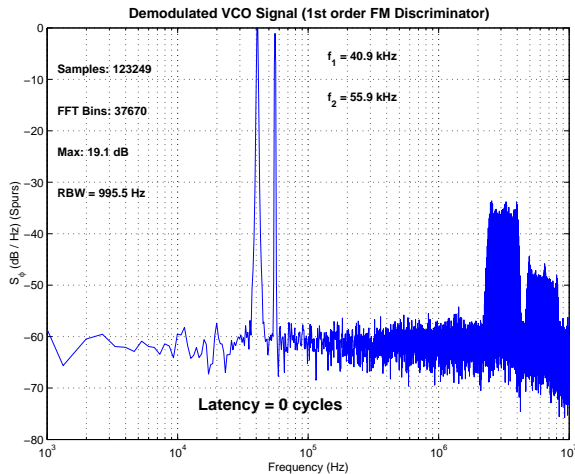


Fig. 11. Downconverted two-tone spectrum using 1st order FM discriminator

The FM discriminator has been layouted by hand and requires an area less than 0.015 mm² on the test chip. No measurement results are available yet.

VII. CONCLUSIONS

An area efficient method for the built-in self test of integrated RF transmitters has been presented that relies entirely on digital components. Multi-tone stimuli are generated with a compact generator utilizing lossless digital integrators and upconverted using the sigma-delta modulation transmit PLL. The FM /PM modulated RF signal is downconverted and digitized using a digital FM discriminator. This test architecture does not interfere with critical RF signal paths as the signal generation and demodulation is performed entirely in the digital domain.

VIII. OUTLOOK

A digital on-chip spectral analysis of the demodulated bit stream will be the next step to allow a complete BIST, reducing even further the requirements for costly RF production test equipment. Built-In Self Calibration (BISC) strategies can also be implemented with this setup to increase the yield and to make the circuit more robust against environmental variations. If necessary, the resolution of the integrated FM discriminator can be improved by increasing the order or the sampling frequency.

ACKNOWLEDGMENT

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