

# Built-In Self-Test (BIST) für RFICs

EEEfCOM 2006

**Infineon**

**Christian Munker**  
Infineon Technologies AG



Never stop thinking.

**Motivation for new RF test concepts**

**Time domain RF BIST**

**Frequency domain RF BIST**

**RF Loopback Test**

**Conclusion**

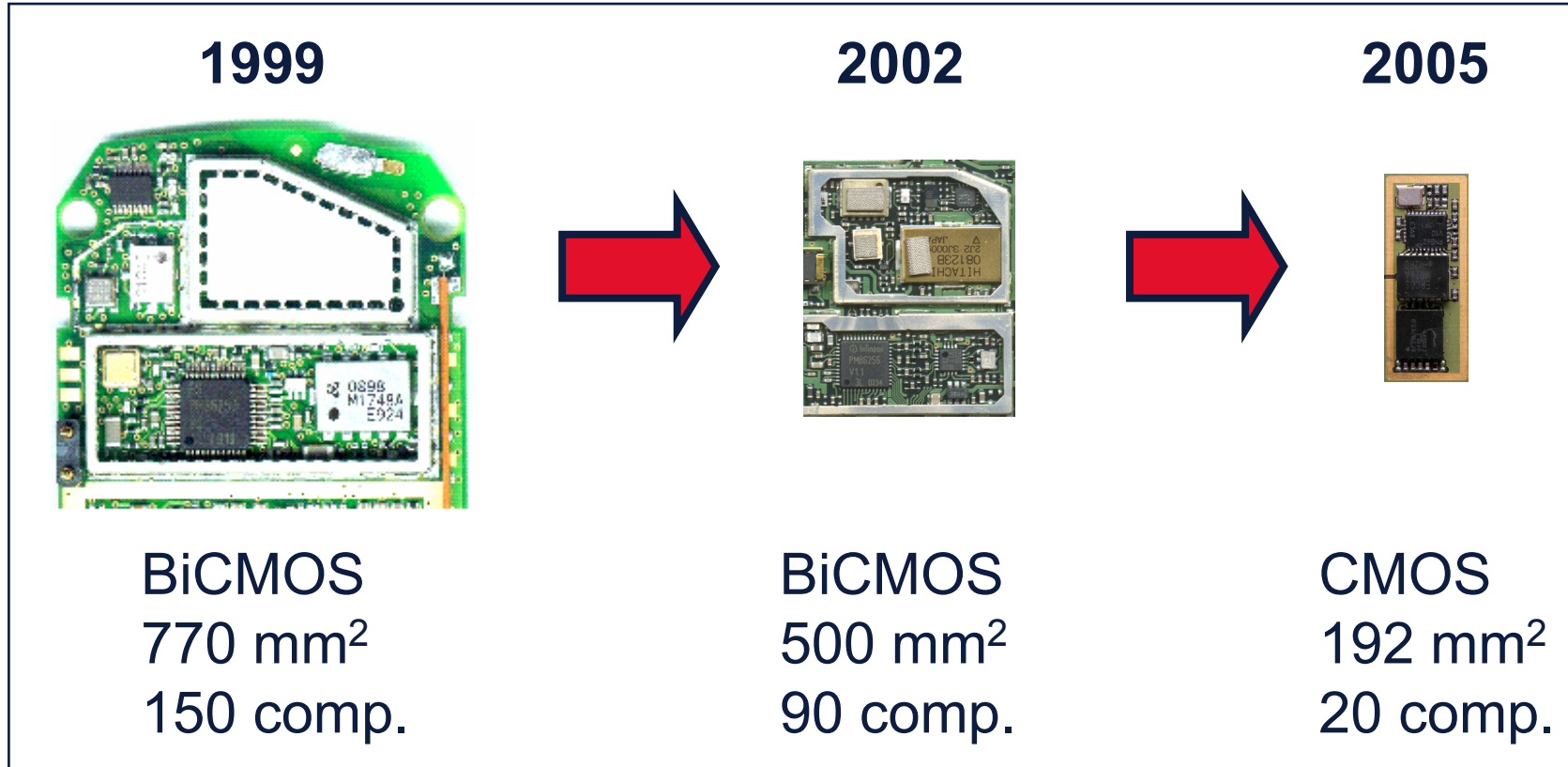
**BIST für RFICs**

**Christian Mürker**  
Infineon Technologies

29-June-2006



## Development of IFX RF subsystem (GPRS / EDGE)



**Trend:** Low cost, small form factor, more features



- Lower costs
- Better shrink potential
- Better integration capabilities
- More signal processing possibilities

**CMOS**



**CMOS is becoming THE mainstream RF  
technology!**

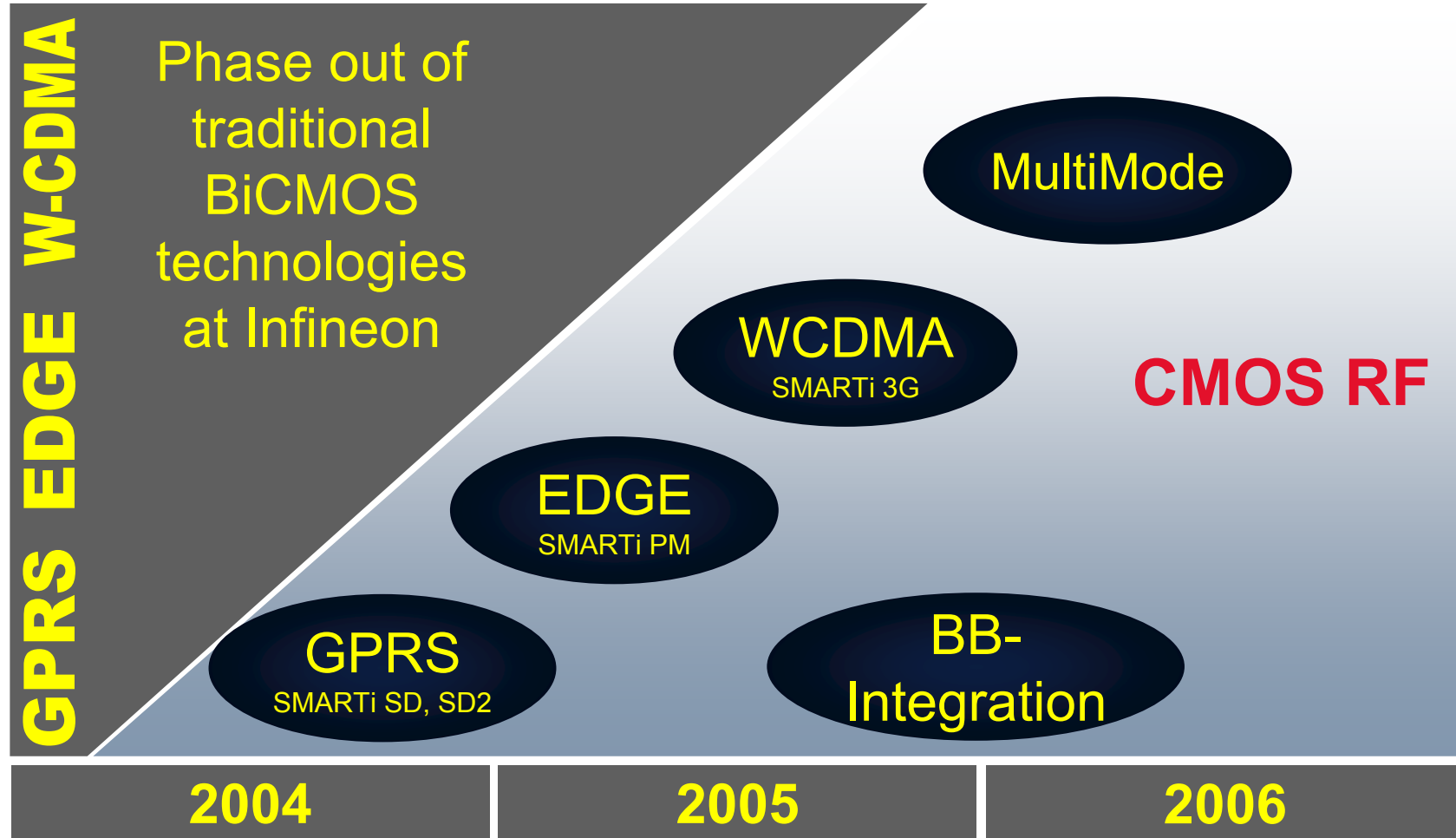


## Pros and Cons of CMOS RF

- + Fast enough for most RF applications
- + Reaches technology nodes ~18 months earlier than BiCMOS
- + Higher degree of integration possible
- Worse flicker noise and parameter spread
- Low  $g_m / I$  ratio

⇒ **New, mainly digital architectures** are needed to make the most of CMOS Technologies!





BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006



- **System-On-Chip:** more system tests have to be performed by chip maker
- **Falling production costs** vs. **Increasing test costs**  
[smaller chips] [more tests]
- **RF – tests are slow** ( $\Rightarrow$  expensive!) because of demodulation / spectral analysis / averaging on ATE

Growing contribution of test costs to production costs!!!

BIST für RFICs

Christian Munker  
Infineon Technologies

29-June-2006



# Critical Productiontests for RF Transmitters

Test	Challenge	BIST
VCO / Divider Functionality	<ul style="list-style-type: none"> <li>- <b>No direct access</b></li> <li>- <b>Lots of failure modes (multiple VCO – Bands and division ratios)</b></li> </ul>	<b>Time Domain</b>
Modulation Spectrum (Mask Conformity)	<ul style="list-style-type: none"> <li>- <b>Long averaging times</b></li> <li>- <b>Complex signal analysis</b></li> </ul>	<b>Frequency Domain</b>
PLL Loop Bandwidth	<ul style="list-style-type: none"> <li>- <b>No direct access</b></li> </ul>	<b>Frequency Domain</b>
Out-of-Band Spectrum (Phase Noise, Spurs)	<ul style="list-style-type: none"> <li>- <b>Long averaging times</b></li> <li>- <b>Dynamic range</b></li> </ul>	???
Output Power	<ul style="list-style-type: none"> <li>- <b>Matching</b></li> <li>- <b>Calibration</b></li> </ul>	???

BIST für RFICs

Christian Munker  
Infineon Technologies

29-June-2006



# Targets for RF IC BIST / BISC

- Speed up of RF test
- No interference with critical RF paths on-chip
- Little area overhead
- No additional yield losses by test circuitry
- Testable test circuitry

**Modern CMOS technologies (130nm → 65 nm) favor digital over analog implementations**



**Mainly digital implementation of BIST circuits!**

**BIST:** Built-In Self Test

**BISC:** Built-In Self Calibration



Motivation for new test concepts

**RF Testconcepts in the time domain**

RF Testconcepts in the frequency domain

RF Loopback Test

Conclusion

BIST für RFICs

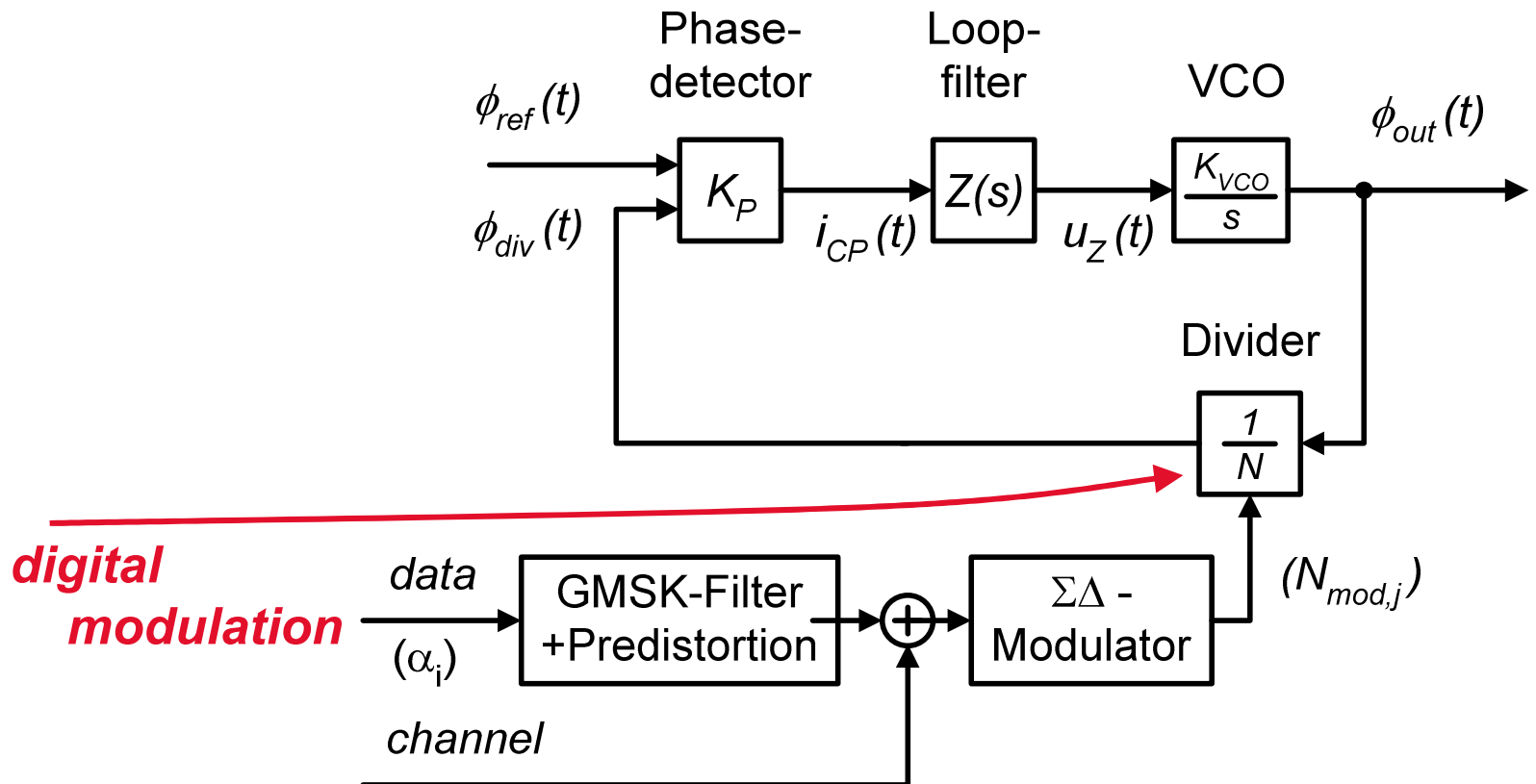
Christian Mürker  
Infineon Technologies

29-June-2006

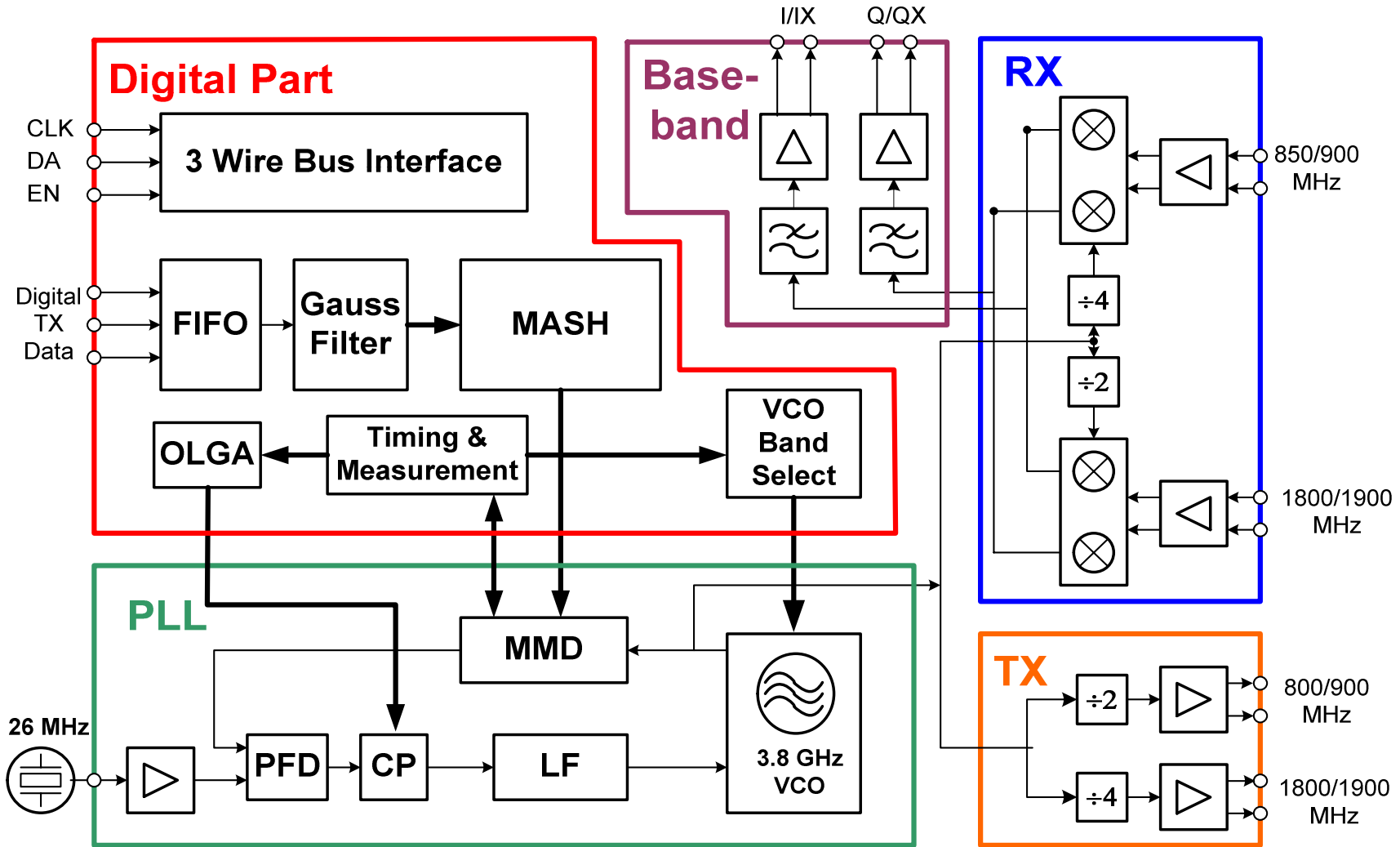


# Example: Sigma-Delta (SD) Modulation Transmit Architecture

- Mainly digital architecture  $\Rightarrow$  well suited for CMOS
- No mixer required  $\Rightarrow$  robust against PA leakage



# GPRS Transceiver with SD-Modulator



BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006



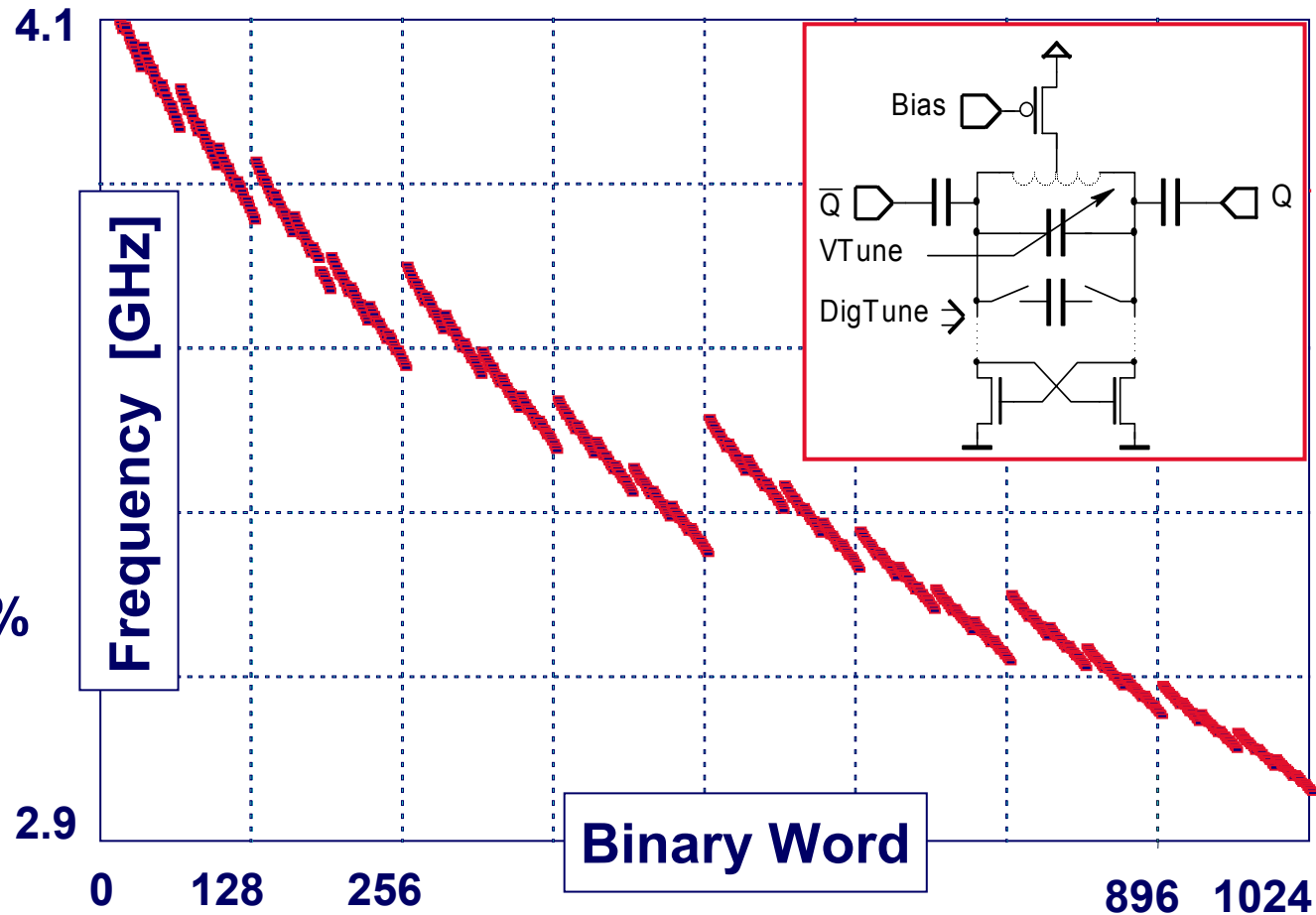
- **Wide VCO tuning range** to compensate for CMOS process variations
- **Low, well controlled VCO gain** to reduce noise contribution
  - ⇒ **Digital pretuning with automatic band selection**
- **Precise control** analog loop characteristic required (max.  $\pm 10\%$  deviation) for digital modulation
  - ⇒ **Automatic digital open loop gain adjustment**

- + **Trade analog precision for digital complexity**
- + **Additional circuitry must be tested**
- + **Additional circuitry can also improve testability!**



# VCO with 10 Bit Digital Pretuning

- **MOS** tuning elements
- Wide tuning range:  
**1200 MHz**
- Low VCO Gain:  
**60 MHz/V  $\pm$  10%**



BIST für RFICs

Christian Munker  
Infineon Technologies

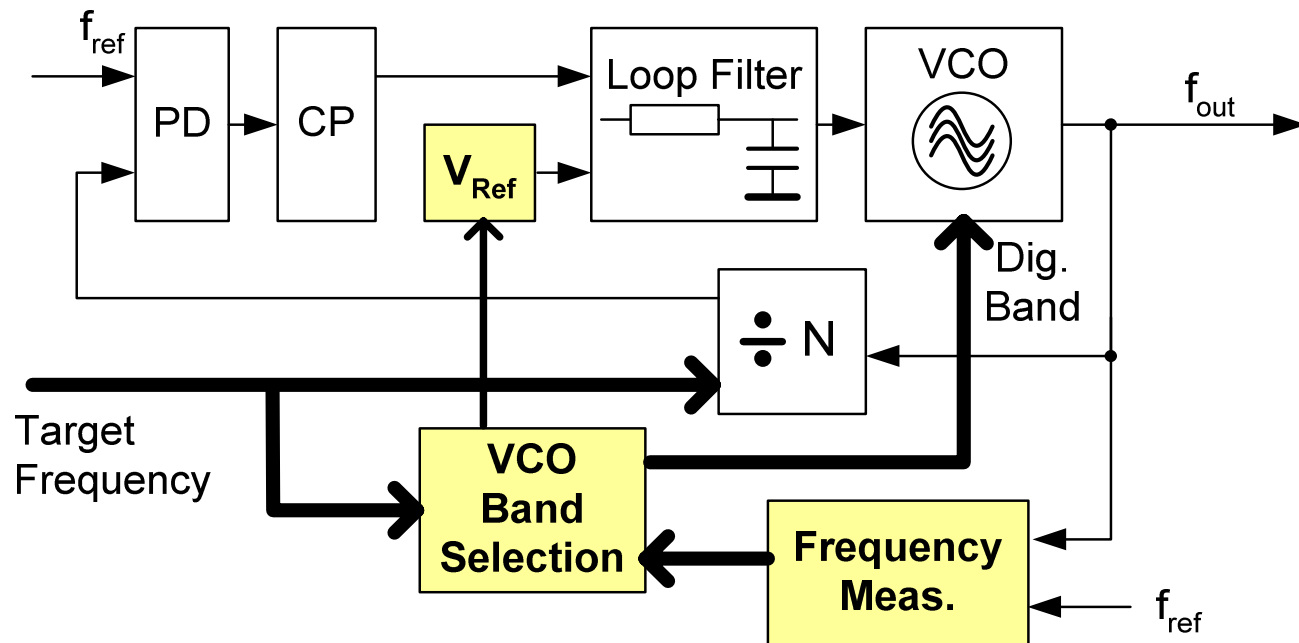
29-June-2006



- ⇒ No expensive technology options (e.g. for varactor)
- ⇒ Large tuning range with digital band selection
- ⇒ Low, well-defined VCO gain for analog tuning

## On-chip frequency measurement:

- select optimum band (BISC)
- characterize VCO frequency range (BIST)



⇒ **Built-In Self-Calibration (BISC) enables Built-In Self-Test (BIST) and vice versa**





Motivation for new RF test concepts

Time domain RF BIST

**Frequency domain RF BIST**

RF Loopback Test

Conclusion

BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006



# Why Frequency Domain RF BIST?

---

- Wireless circuits and systems are specified and must be tested in the frequency domain
- Translation of time-domain measurements into the frequency domain (e.g jitter  $\Rightarrow$  phase noise) is error prone and time consuming
- On-chip frequency domain characterization can be used for new self-calibration schemes (BISC)!

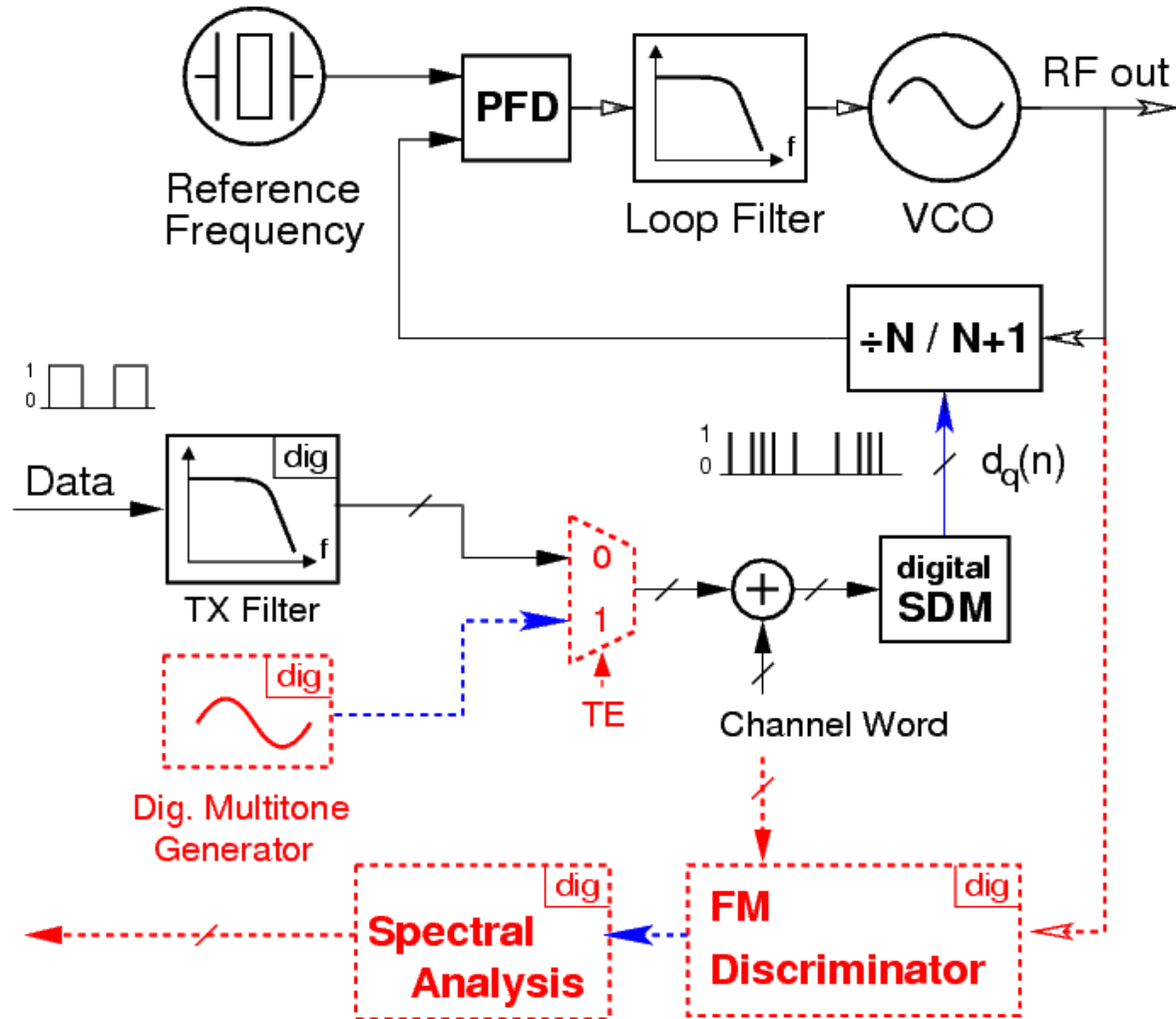
BIST für RFICs

Christian Munker  
Infineon Technologies

29-June-2006



# Overview: On-Chip Frequency Response Analysis



**On-chip digital multitone RF generator and narrowband spectral analysis enable frequency response analysis**



Motivation for new RF test concepts

Time domain RF BIST

**Frequency domain RF BIST**

**On-chip RF stimulus generation**

On-chip RF response analysis

RF Loopback Test

Conclusion

BIST für RFICs

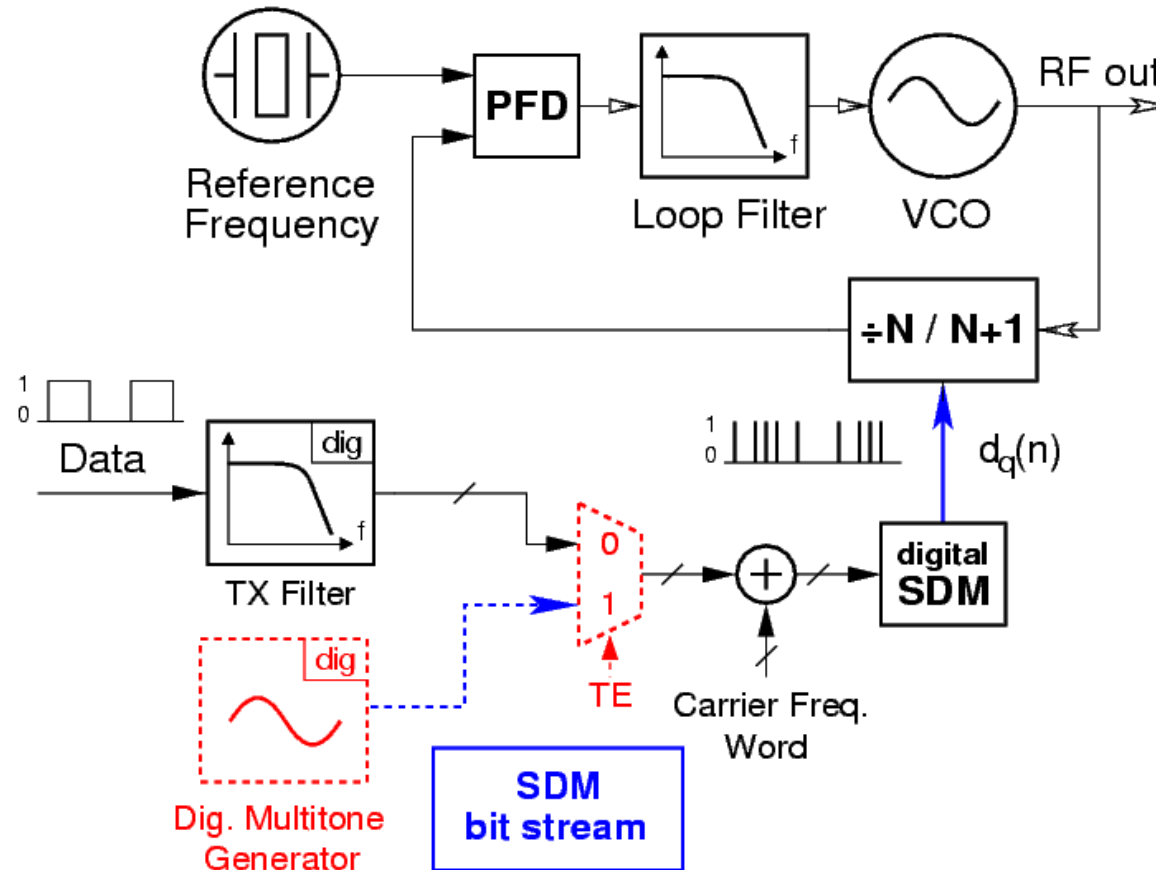
Christian Mürker  
Infineon Technologies

29-June-2006

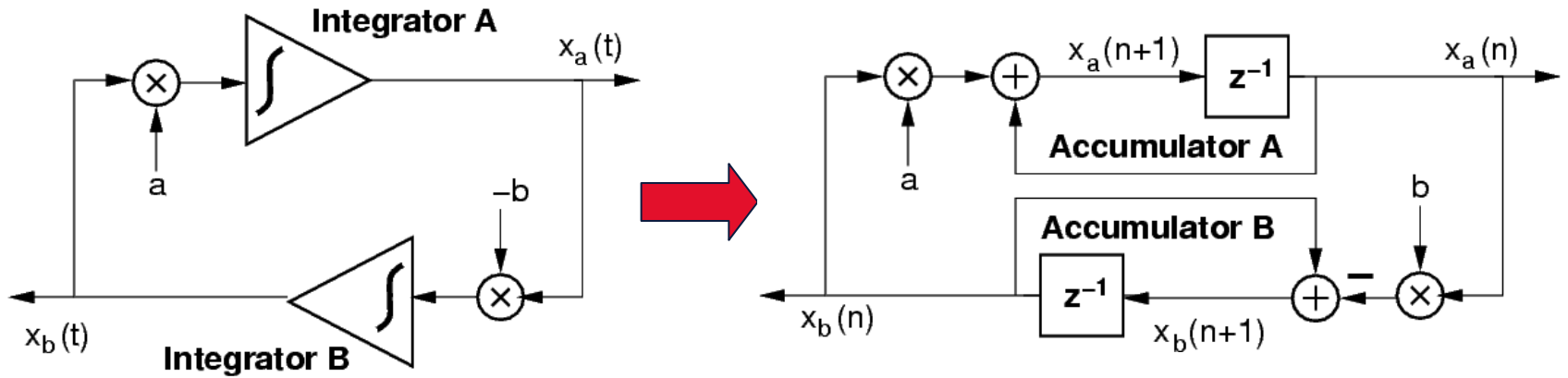


# On-Chip RF Stimulus Generation

- Test-tones are generated digitally
- D/A Conversion and upconversion is performed in TX Sigma-Delta Modulated PLL



# Digital Oscillator Using Lossless Digital Integrators



BIST für RFICs

Christian Munker  
Infineon Technologies

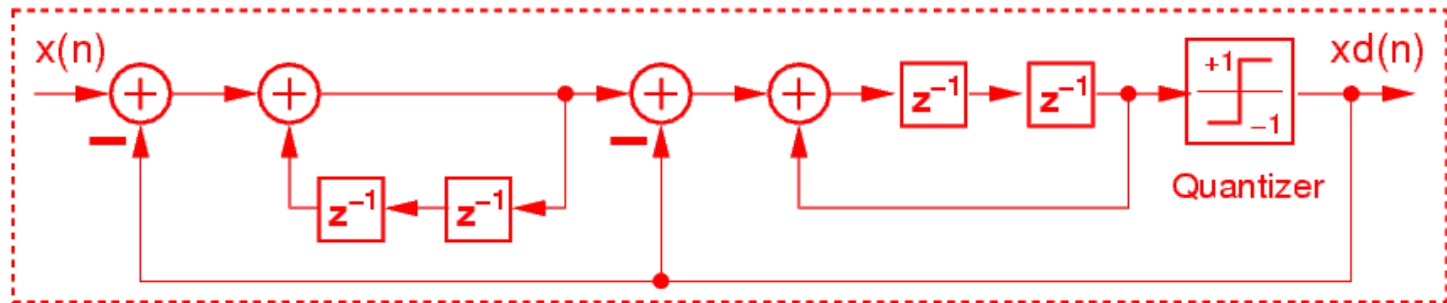
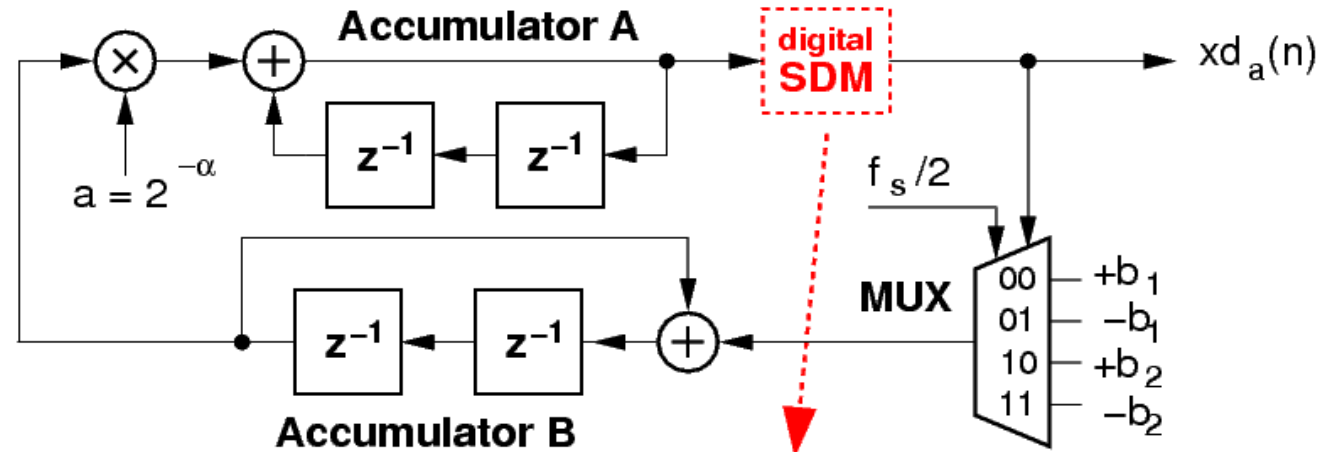
29-June-2006

## Resources per Tone:

- 2 N x N-Bit Multipliers
- 2 N-Bit Accumulators



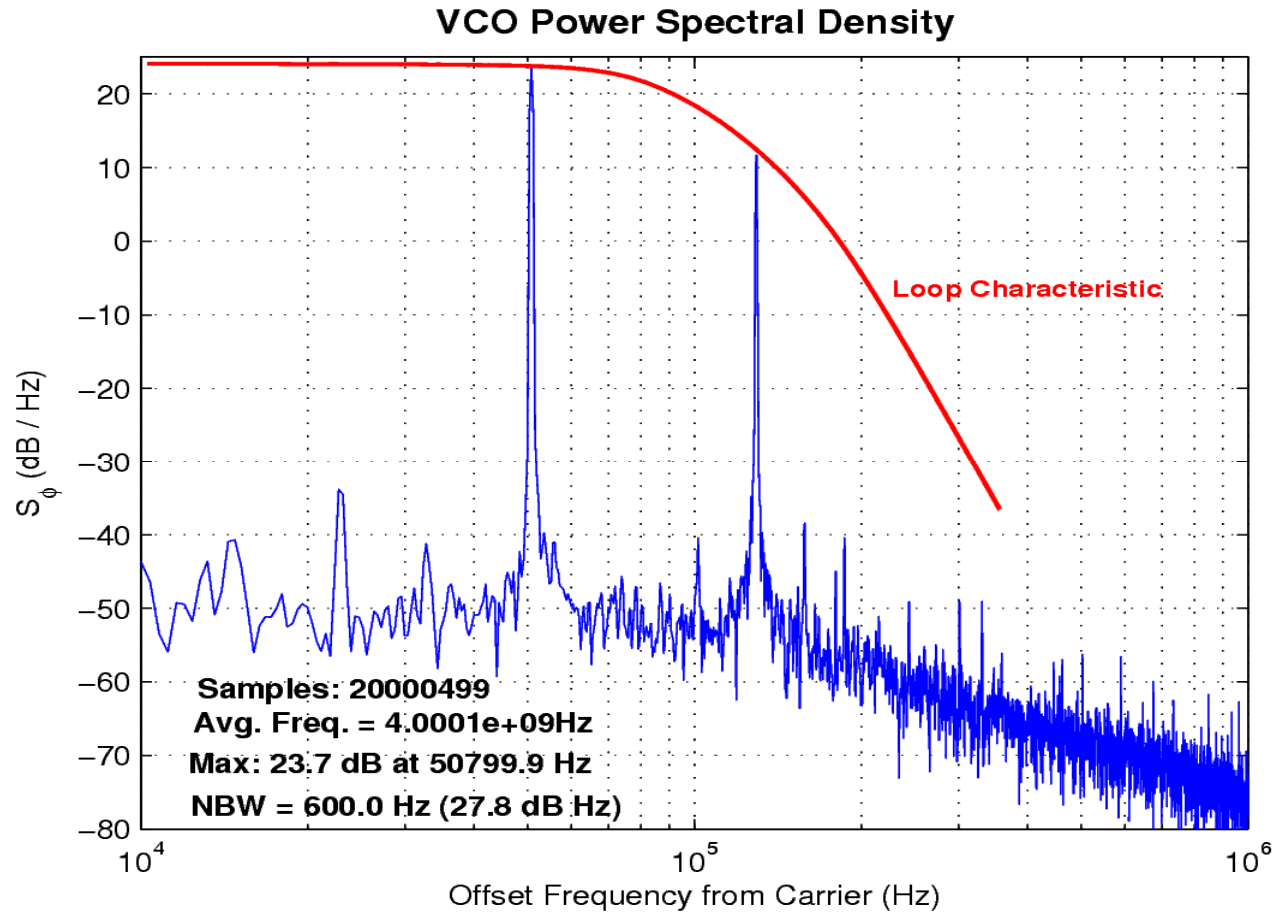
# Digital Multi-Tone Generator Using SDM Attenuator



- SDM to replace multiplier by multiplexer (SDM attenuator)
  - Time-division multiplexing to share hardware between tones
  - 4 extra N-Bit registers needed per tone
- ⇒ **Only 0.02 mm<sup>2</sup> chip area for 2 tones with 15 bit resolution**



# Two-Tone Spectrum at PLL Output



BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006



Measure Loop Characteristics Using Two-Tone Signal

Motivation for new RF test concepts

Time domain RF BIST

**Frequency domain RF BIST**

On-chip RF stimulus generation

**On-chip RF response analysis**

RF Loopback Test

Conclusion

BIST für RFICs

Christian Munker  
Infineon Technologies

29-June-2006



- RF signal has to be converted into base band domain and digitized for on-chip analysis
- RF loop-back does not work (only one PLL)
- Additional down-conversion mixer / BB ADC is too large and „too analog“
- What else?



BIST für RFICs

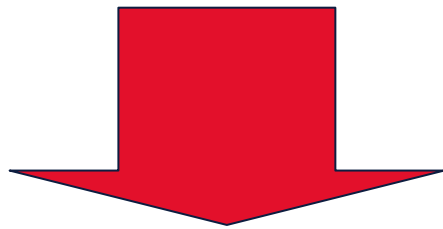
Christian Mürker  
Infineon Technologies

29-June-2006



# Exploitation of RF TX Signal Properties

- Rail-to-rail signal on RF CMOS ICs
- High spectral purity
- Small signal bandwidth
- Carrier frequency is known on-chip
- Only FM / PM modulation (for PLL test)



**Apply Digital Techniques!**

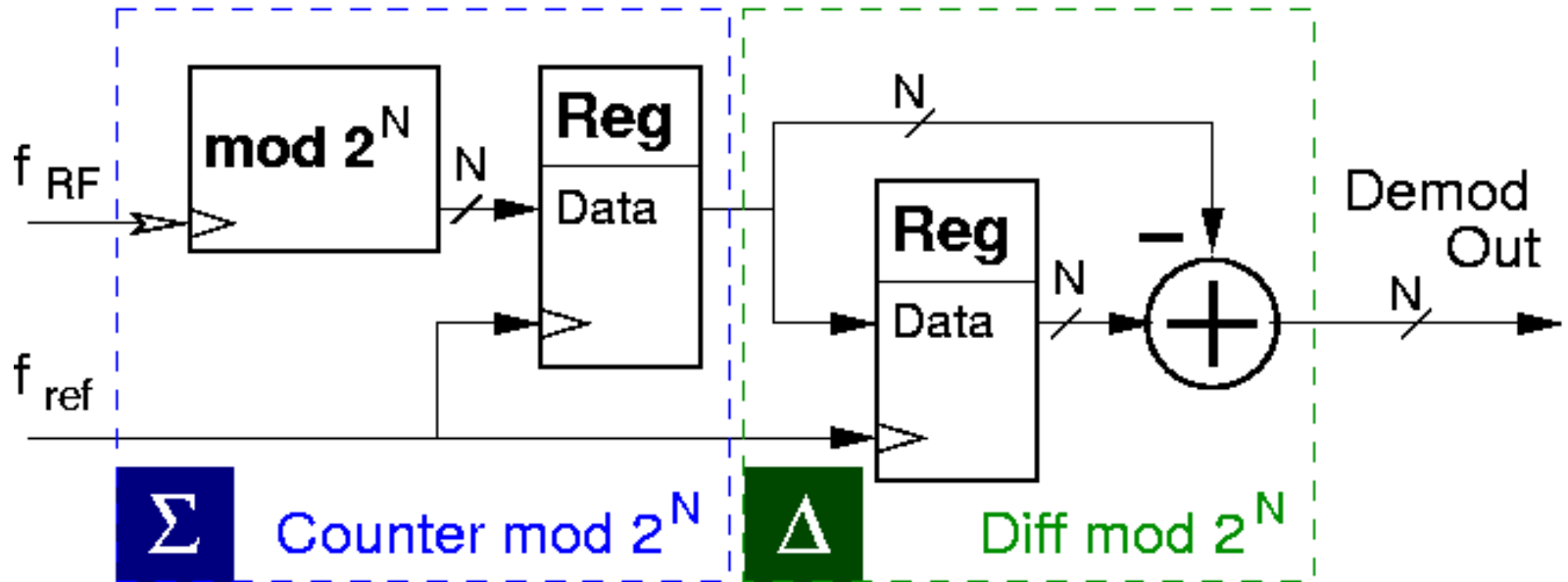
**Frequency- or Time-to-Digital converter**

BIST für RFICs

Christian Munker  
Infineon Technologies

29-June-2006

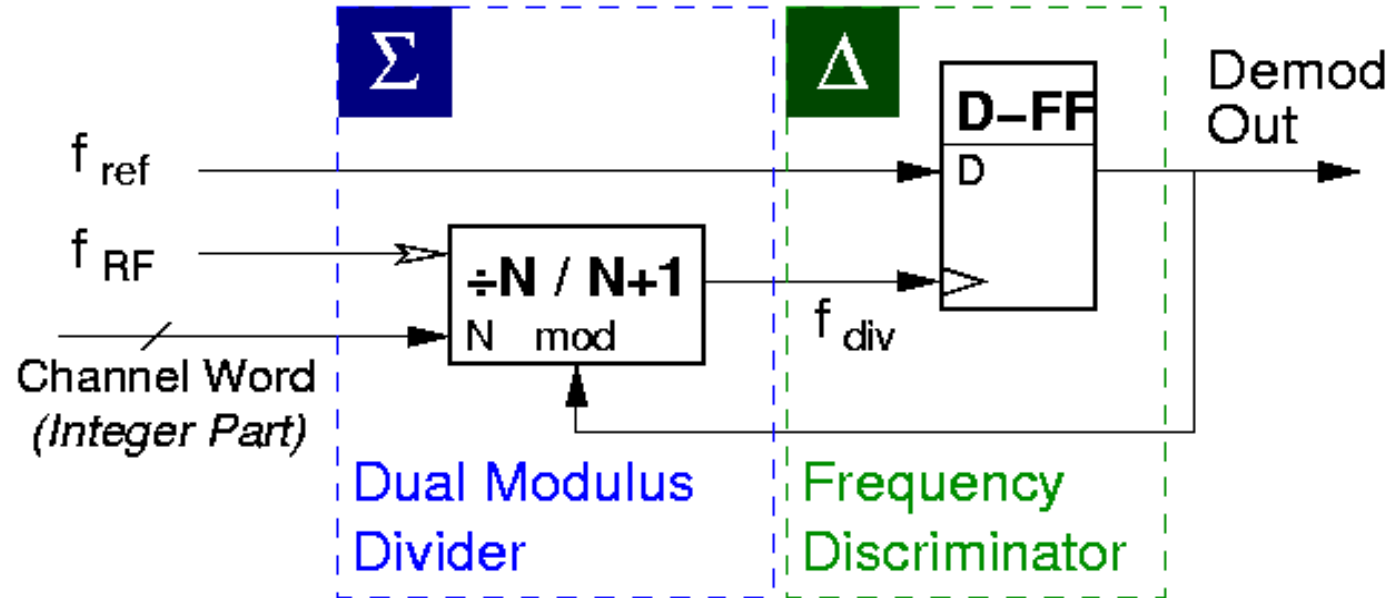




- high-speed synchronous counter required
- precise latching of counter at RF speed required

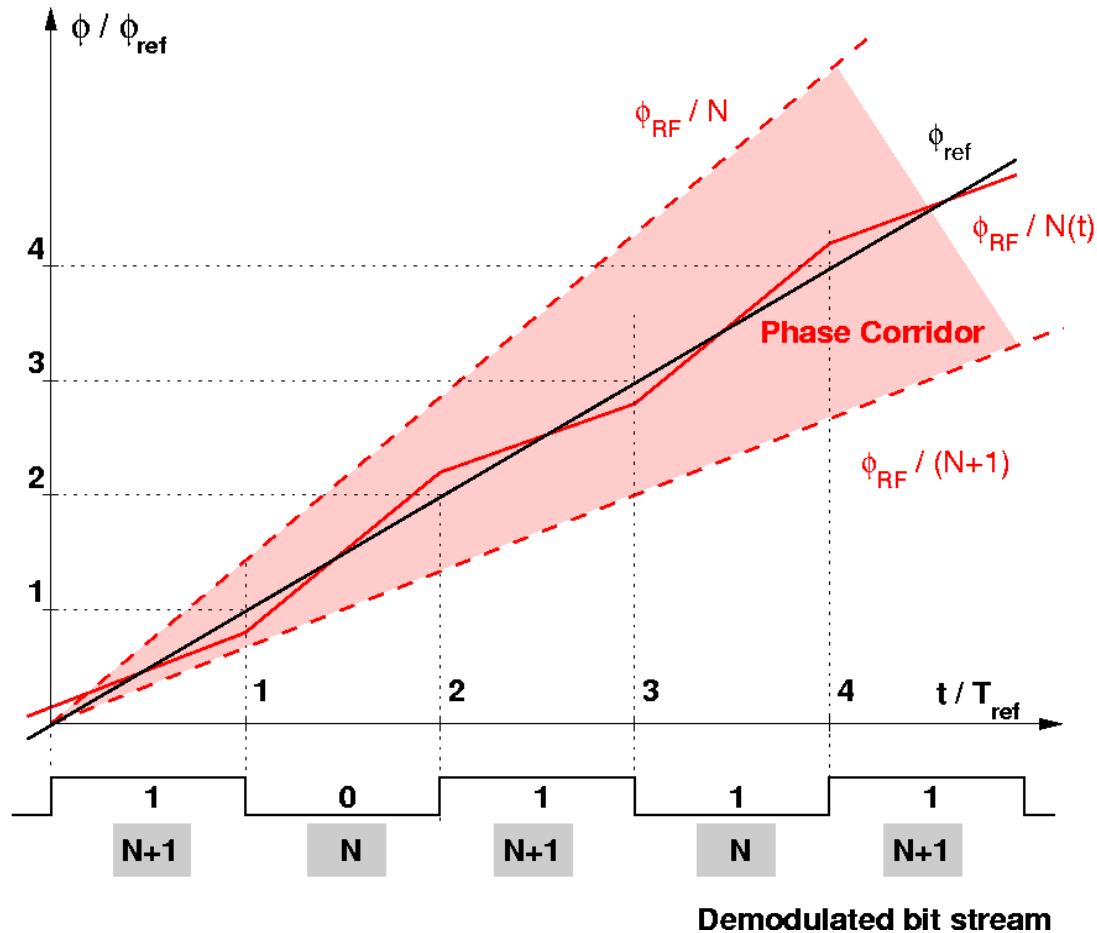


# 1st Order Frequency Sigma-Delta Conversion (FSDM)



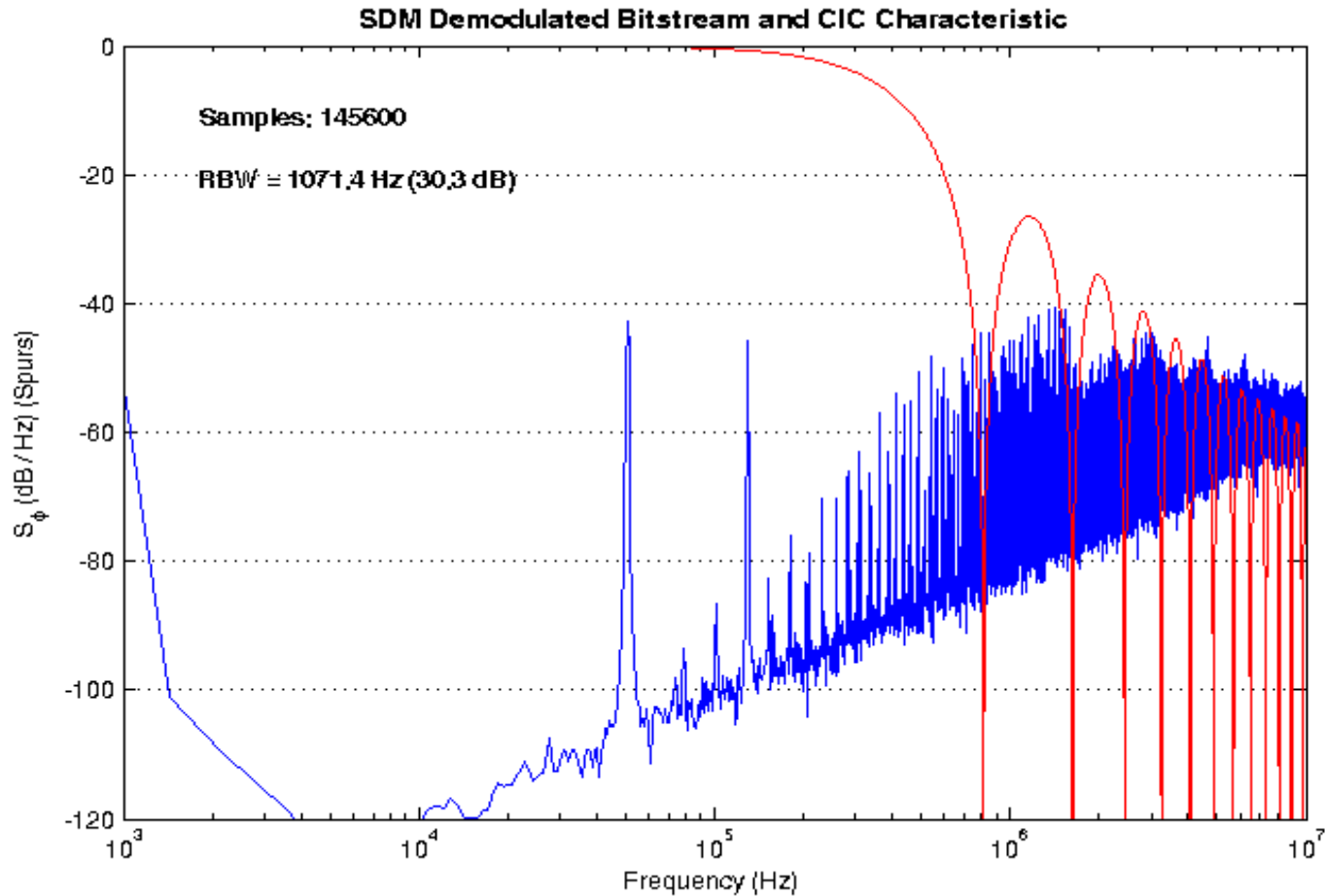
- + building blocks can be copied from PLL
- + no high-speed latching required
- re-synchronisation to  $f_{ref}$  needed (not a big problem)





- Dual Modulus Divider operates as integrator + quantizer
- D-FF compares divided RF phase and reference phase

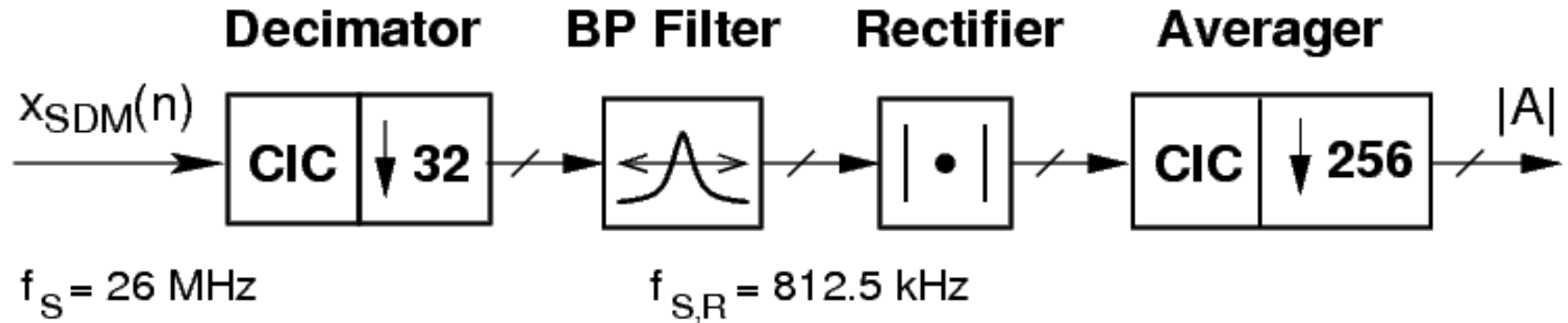




- Quantization noise grows with 20db/dec. (1st order SDM)
- Decimation filter needs to be at least 2nd order



# Structure of Narrowband Filter

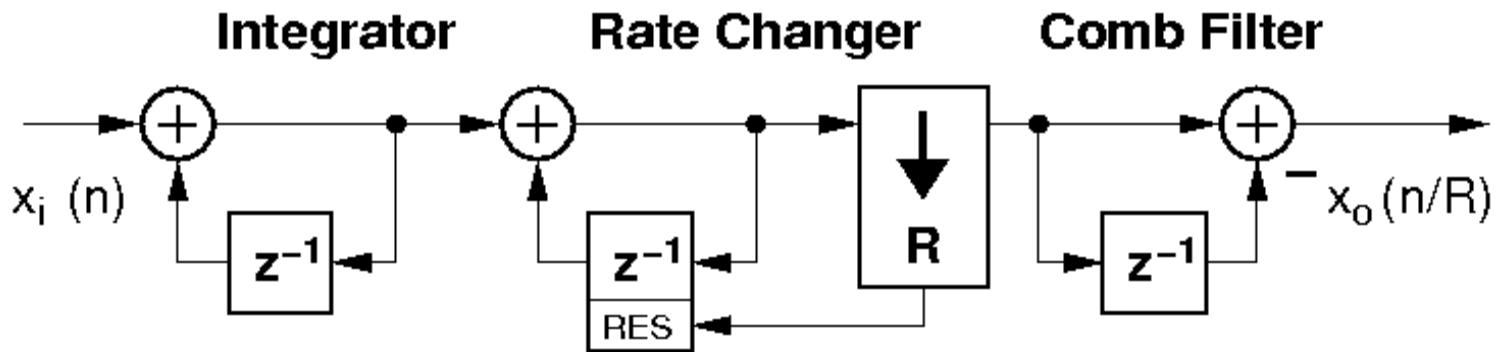


- Spectral analysis is performed by narrow-band filtering instead of FFT
- Bands of interest are measured one after the other
- Amplitude can be read via 3WB as static word
- Less than  $0.03\text{mm}^2$  for 4<sup>th</sup> order programmable BP with a freq. resolution of 300 Hz



# 2nd Order CIC Filter for Downsampling

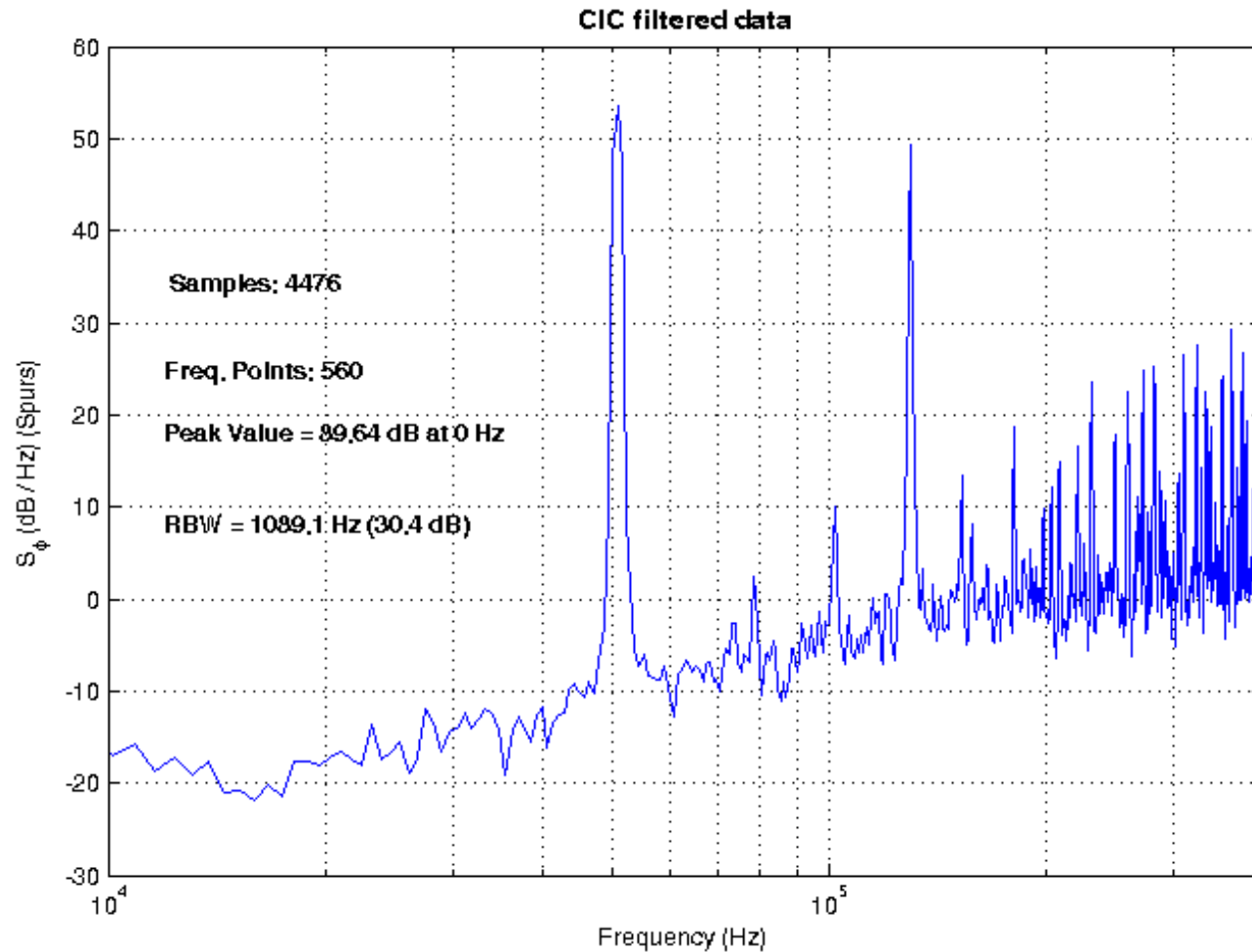
**Downsampling** : Process of resampling at a lower sample rate, including an antialias filter followed by a decimation.



CIC: Cascaded Integrator-Comb Filter

- + Multiplier-less structure for compact filter implementation
- Only weak low-pass characteristic

# Spectrum After Decimation Filter



- Reduced sampling rate  $26 \text{ MHz} / 32 = 812.5 \text{ kHz}$

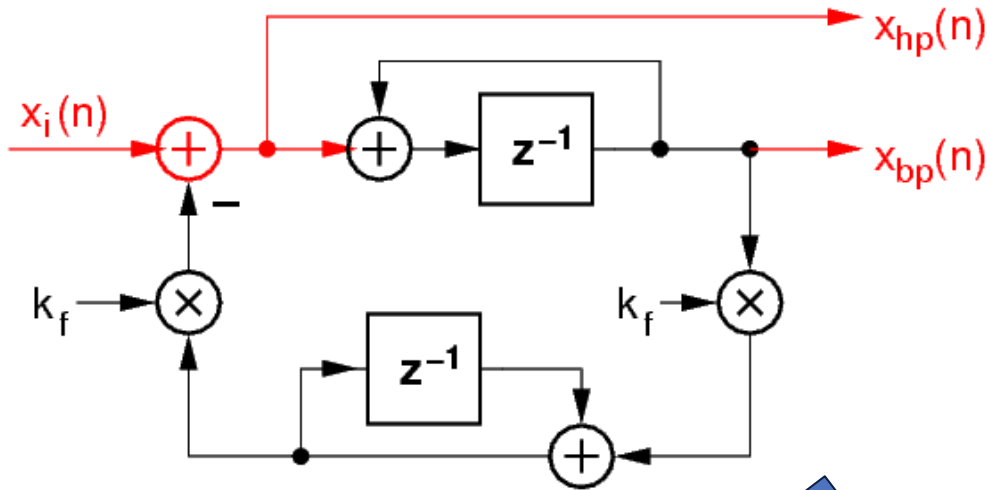
BIST für RFICs

Christian Munker  
Infineon Technologies

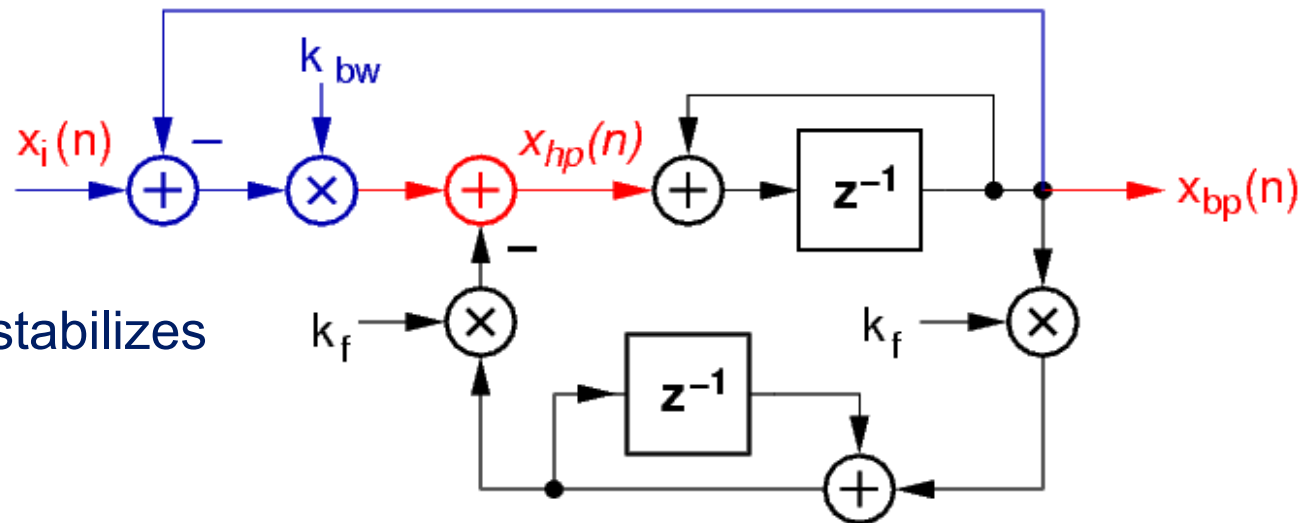
29-June-2006



# Digital Integrator as Programmable Bandpass-Filter



Purely imaginary poles  $\Rightarrow$  system oscillates!



Damping ( $k_{BW}$ ) stabilizes system!



# Advantages of Lossless Digital Integrator (LDI) Filters

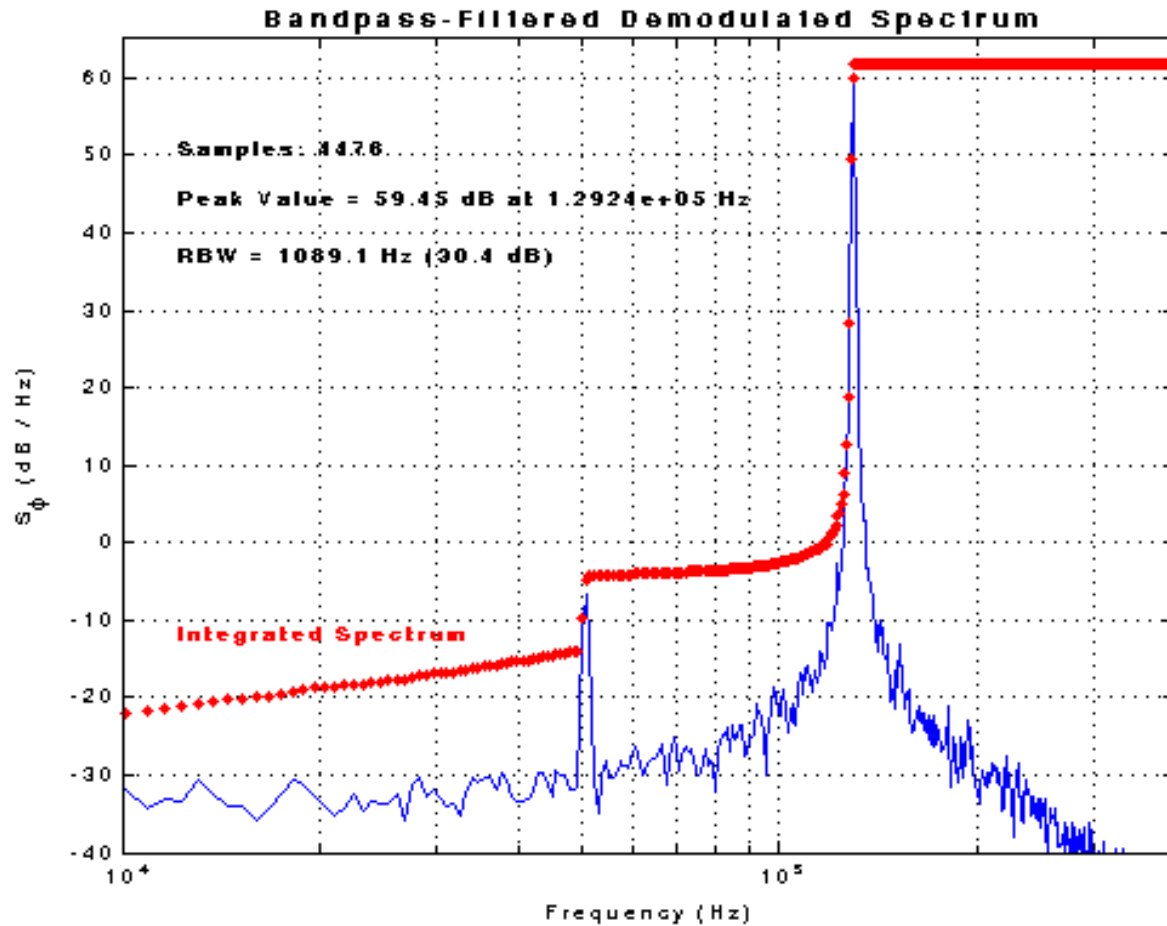
- Insensitive against coefficient truncation (only 9 bit wide!)
- Truncation error only influences center frequency, not the noise performance or stability
- Center frequency is set with only 1 parameter
- Simple structure and low sampling rate allows serialization – only 1 multiplier for 4th order bandpass!
- Parallel multi-tone analysis is possible with little extra effort

**Lossless Digital Integrator (LDI)** structures enable compact and robust digital filters and oscillators

- limited flexibility, use WDF or “classical” FIR / IIR filters for special frequency response requirements



# Spectrum at the Bandpass Output



BIST für RFICs

Christian Münker  
Infineon Technologies

29-June-2006



Integrated spectrum indicates sufficient SNR for amplitude measurement

Motivation for new RF test concepts

Time domain RF BIST

Frequency domain RF BIST

**RF Loopback Test**

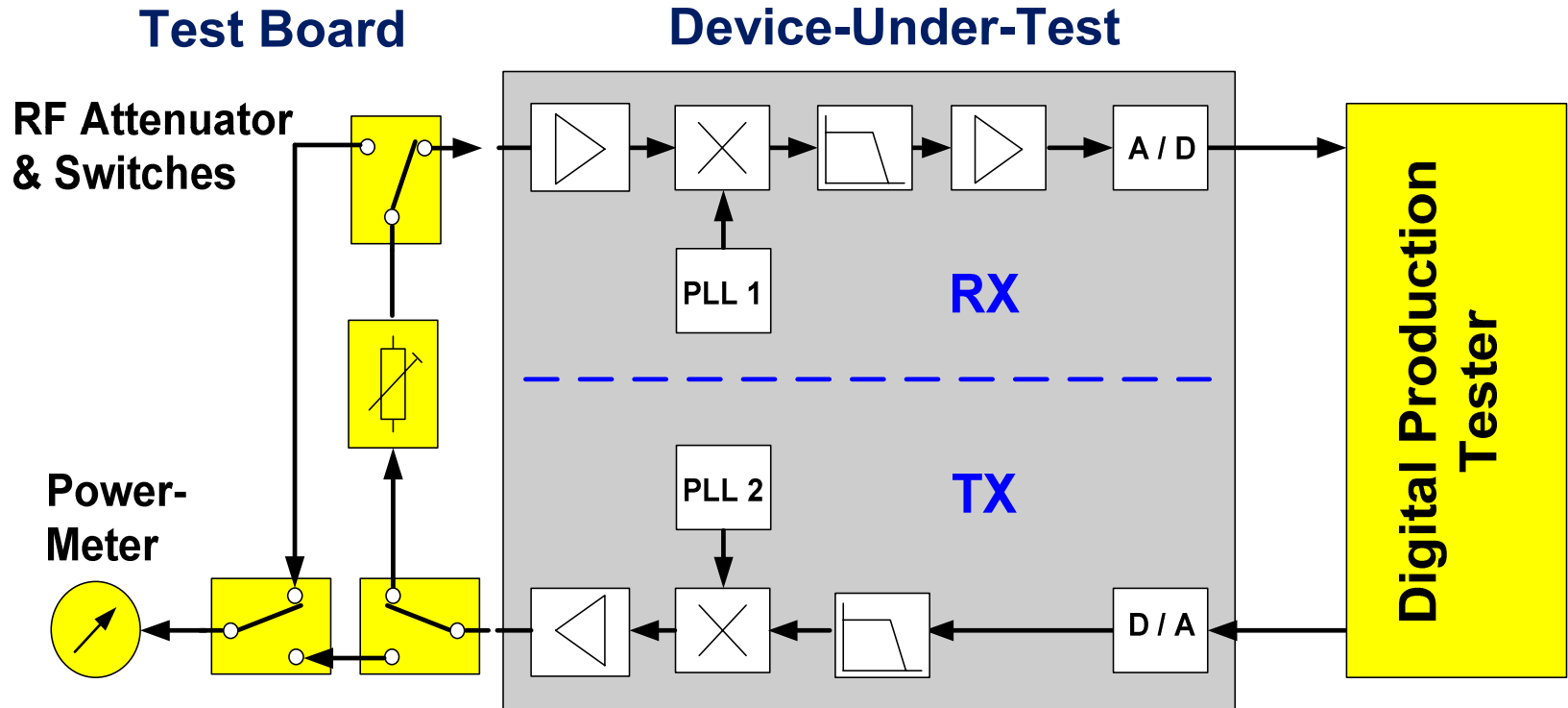
Conclusion

BIST für RFICs

Christian Mürker  
Infineon Technologies

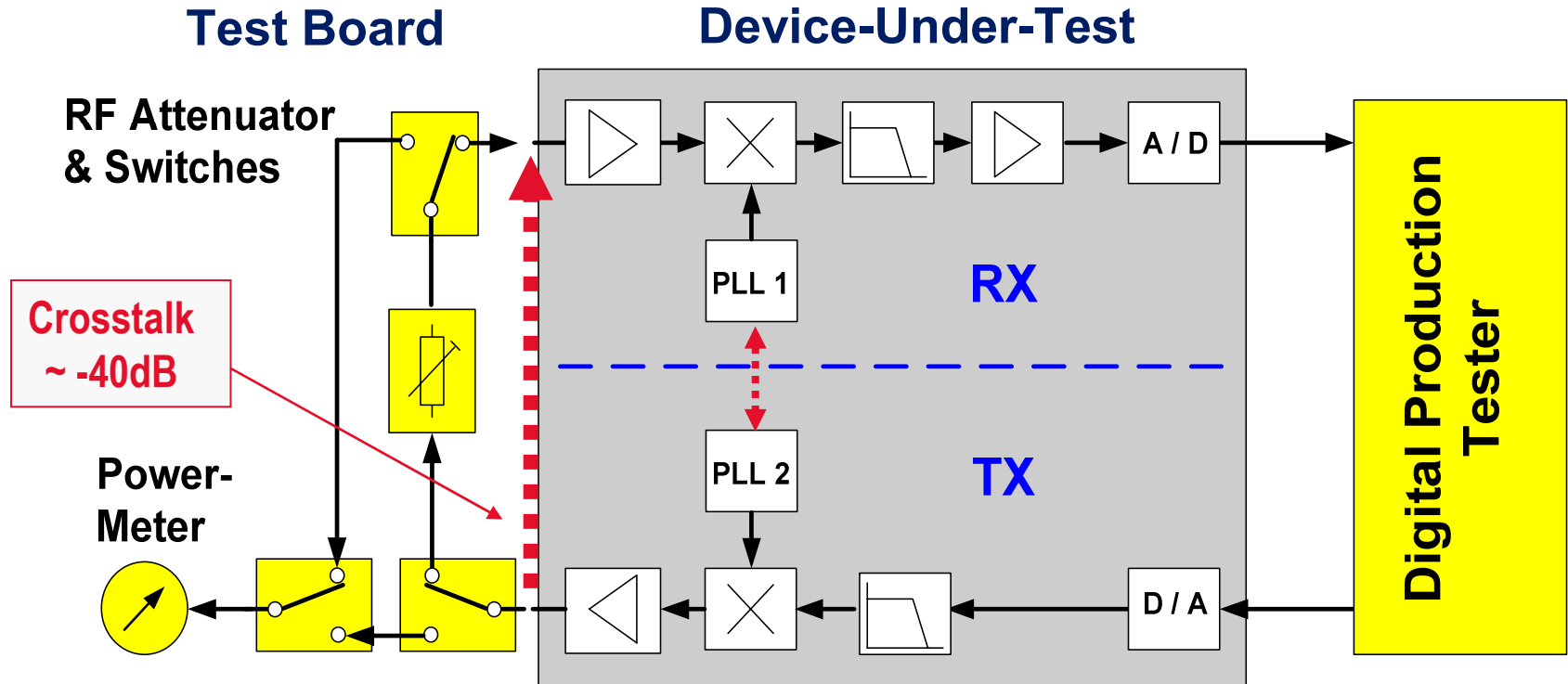
29-June-2006





- TX RF signal is down-converted by on-chip receiver
  - Digital stimuli and response analysis is performed on *digital* production tester
- ⇒ **no special RF tester required!**





- **Unwanted crosstalk** between TX and RX limits dynamic range
- **Frequency division duplex systems:** common frequency for RX and TX?
- **TDMA systems** (e.g. GSM, WLAN): independent PLLs available?



## Further drawbacks of RF Loop-Back Test

---

- **TDMA systems** (e.g. GSM, WLAN): Simultaneous operation of RX and TX possible?
  - Power Consumption
  - Crosstalk
  - Independent PLLs available
- **Matching RX / TX specifications?**

**RF Loop Back Test** is not suitable for extensive production test in most cases. Coarse functional test may be feasible.



Motivation for new RF test concepts

Time domain RF BIST

Frequency domain RF BIST

RF Loopback Test

**Conclusion**

BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006



- Digital RF architectures are a prerequisite for low-cost CMOS solutions by providing built-in self-calibration (BISC) functionality
- Built-in self calibration enables built-in self test (BIST)
- High integration densities allow powerful, yet compact digital calibration and self-test features
- DSP functionality enables frequency domain BIST for direct verification of spectral specifications

## Examples:

- Two-tone frequency modulated RF signals are generated with a completely digital test oscillator
- FM RF signals are demodulated and analyzed with a digital FM discriminator and narrowband filter
- Oscillator and discriminator allow measurement of PLL spectral parameters like loop characteristic and sideband power



---

# Danke für Ihre Aufmerksamkeit!

**BIST für RFICs**

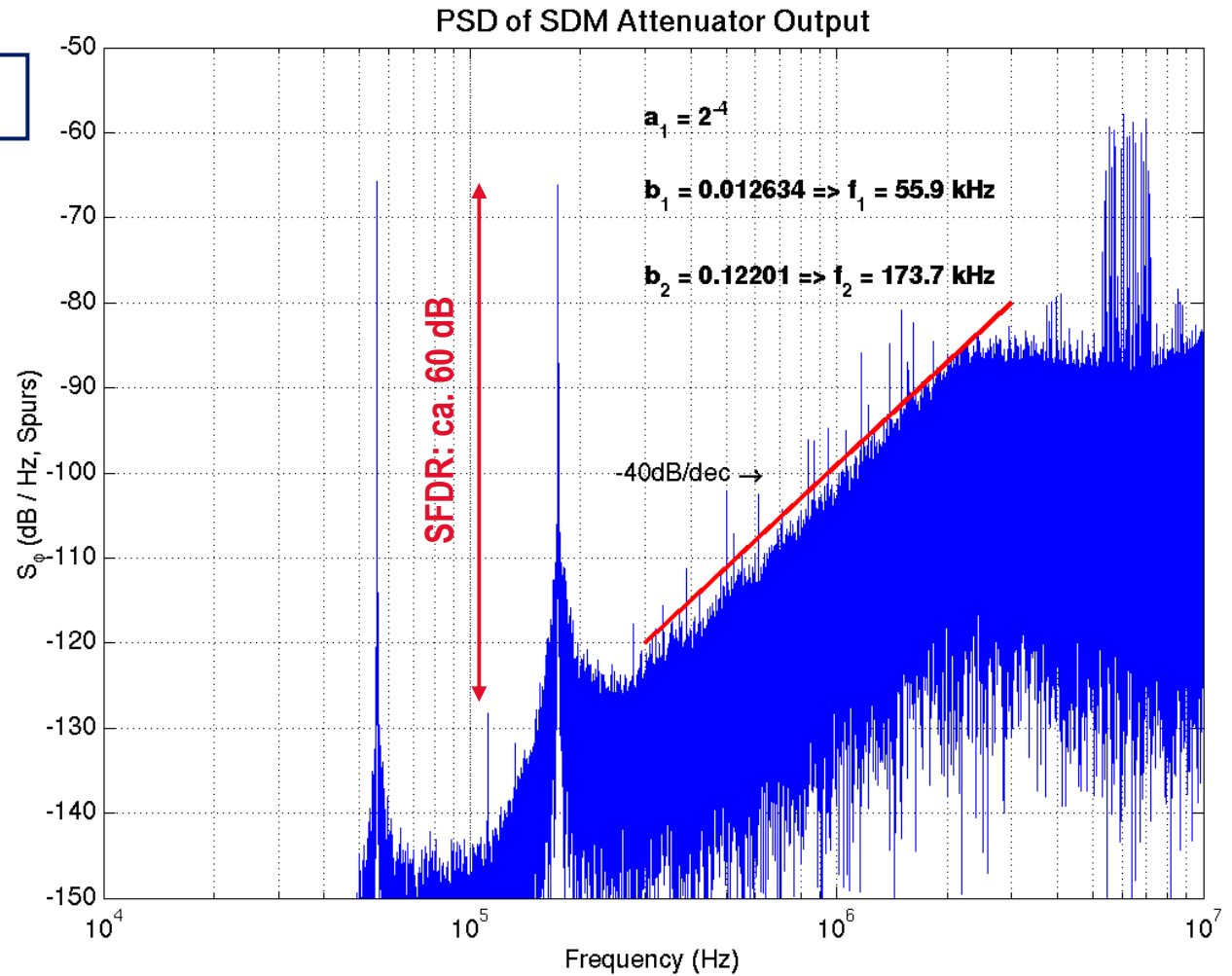
**Christian Munker**  
Infineon Technologies

29-June-2006



# Two-tone Spectrum of Digital Sine Generator (SDM Out)

**N = 15 bits**



BIST für RFICs

Christian Mürker  
Infineon Technologies

29-June-2006

