

# RF Built-In Self-Test for Integrated Cellular Transmitters

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**Abstract**—A spectral built-in self test (BIST) solution for integrated cellular RF transmitters is presented that enables on-chip verification of PLL spectral performance. Multi-tone FM test signals with a spurious-free dynamic range (SFDR) of 60 dB are generated without compromising the performance of the RF transmitter itself. The RF signal is demodulated and digitized in an on-chip digital FM discriminator, spectral analysis is performed using digital narrowband filtering. The additional BIST blocks are fully digital and have been implemented on a chip area of only 0.05 mm<sup>2</sup> in a 130 nm CMOS technology. The test blocks allow fast measurement of PLL frequency response, level of spurious sidebands and in-band phase noise down to -80 dBc without external test equipment. Catastrophic faults and most parametric faults can be detected as long as they influence the loop bandwidth or deteriorate spectral performance.

## I. INTRODUCTION

Until a few years ago, production test for RF ICs required a good understanding of RF measurement techniques and equipment but little Design-for-Test (DfT) or even BIST capabilities due to the low device complexity. The advent of mainstream CMOS technologies with transit frequencies exceeding 100 GHz has changed the picture: Fired up by a general trend towards wireless devices, RF ICs have become highly integrated, high volume commodity products for consumer markets with fierce competition and shrinking profit margins. As a consequence, test costs account for a growing percentage of the total production costs, turning DfT and BIST into an economic necessity for RF ICs.

Recently, several loop back test concepts have been proposed for integrated RF transceivers where the on-chip receiver (RX) is reused for demodulating the RF transmit (TX) signal. While loop back concepts look very appealing due to low area overhead, there are some pitfalls for the practical implementation: Most standards use frequency division duplexing, requiring to run either RX or TX path outside the specified frequency range during loop back test. RX and TX path usually have very different requirements concerning dynamic range, distortions etc., preventing a thorough test of both paths. Chips built for time-division multiplex access systems like GSM or Bluetooth are not specified for or even capable of operating RX and TX path at the same time. Additionally, loop back test is an overall

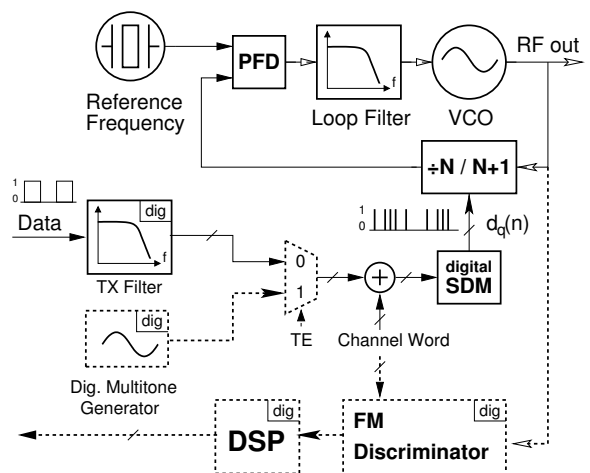


Fig. 1: Fractional-N modulator with BIST blocks (dashed lines)

system test, giving no information on the cause of the failure which is important for yield optimization.

For these reasons, an hierarchical test of the building blocks of an SOC is favored. PLLs are building blocks that are especially hard to test because they are completely embedded in most SOCs with no direct access to their analog ports. This paper presents a novel RF BIST approach for autonomous, specification oriented test of RF PLLs. Spectral parameters like frequency response, in-band phase noise or the level of spurious sidebands can be measured on-chip and compared directly to the component's specification without disturbing performance critical RF paths. The BIST functionality is achieved using robust, digital signal processing blocks with little area penalty due to the high integration density of the 130 nm CMOS technology.

The BIST blocks have been integrated on an RF transmitter utilizing a digital sigma-delta modulator (Fig. 1). This architecture is commonly used for highly integrated RF CMOS transceivers because it is well adapted to CMOS technologies [1].

Section II describes the generation of digital multi-tone signals and section III how to upconvert these stimuli to the RF domain. Section IV shows how to demodulate and digitize the RF signal without analog downconversion or high-resolution ADCs. Section V demonstrates an efficient way for on-chip spectral analysis of the demodulated bit stream by applying digital narrowband filtering.

## II. DIGITAL MULTI-TONE GENERATION

The main building block for generating multi-tone signals is a digital oscillator (Fig. 2), realized with lossless digital integrators (LDI) [2]. LDI based structures are derived from lossless LC - ladder filters; similar to Wave Digital Filters (WDF) they can be implemented with short coefficients. Coefficient truncation errors in LDI based circuits only influence the resonance resp. filter frequency but do not compromise stability or noise performance [3] which makes this principle a good choice for very compact circuits with moderate precision requirements.

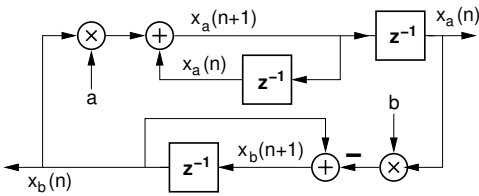


Fig. 2: Principle of LDI oscillator

Analytical expressions for oscillation frequency  $\omega_{sig}$  and amplitude  $x_a$ , depending on sampling frequency  $f_s$ , coefficients  $a$ ,  $b$  and the initial conditions  $x_a(0)$  and  $x_b(0)$ , have been derived in [4]. For  $x_b(0) = 0$  and small coefficients  $|ab| \ll 1$  the following approximations hold true

$$\omega_{sig} = \arccos\left(1 - \frac{ab}{2}\right) f_s \approx \sqrt{ab} f_s \quad (1)$$

$$\phi_a \approx -\arctan\left(\frac{2x_a(0)}{\sqrt{ab}}\right) \approx \pi/2 \quad (2)$$

$$\hat{x}_a \approx \frac{x_a(0)}{\sin \phi_a} \approx x_a(0), \quad (3)$$

showing that amplitude and frequency can be controlled independently. A compact implementation of the oscillator in Fig. 2 is achieved by replacing one multiplier with a fixed bit shifter ( $a = 2^{-\alpha}$ ). The other one is substituted by a sigma-delta attenuator that first converts the  $N$  bit wide data  $x(n)$  into an equivalent oversampled single-bit stream  $xd(n)$  with a Sigma-Delta Modulator (SDM). Multiplication of  $xd(n)$  with the constant coefficient  $b$  then only requires selection of  $+b$  or  $-b$ , depending on  $xd(n)$ .

$L$  tones can be generated in parallel with the same hardware by using time division multiplexing, reducing the effective sampling rate to  $f_{s,eff} = f_s/L$ . This modification requires only four additional registers per tone (Fig. 3) [4]. The quantization noise of the SDM limits the useful signal bandwidth  $BW$  of

the oversampled oscillator. The achievable signal-to-noise ratio  $SNR$  depending on the oversampling ratio  $OSR = f_s/2BW$  is [4]

$$SNR = \frac{\pi^2}{\sqrt{60}} OSR^{-5/2}. \quad (4)$$

The PLL under test has a loop bandwidth of 100 kHz and attenuates quantization noise at higher frequencies. For a two-tone generator ( $L = 2$ ) running with a sampling frequency of 26 MHz, the oversampling ratio is  $OSR = f_{s,eff}/2BW = 13 \text{ MHz}/200 \text{ kHz} = 65$ . The resulting SNR given by (4) is 89 dB.

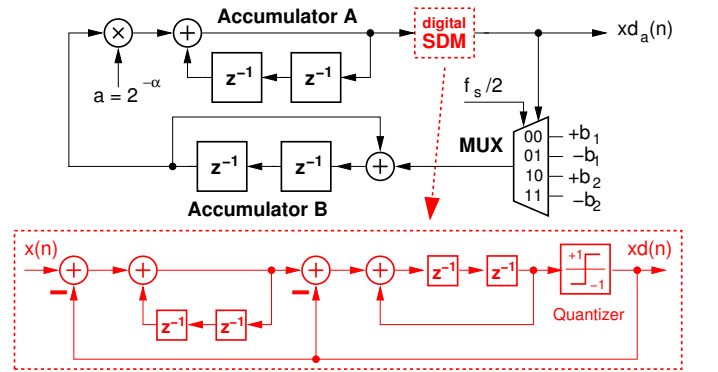


Fig. 3: Two-tone LDI oscillator using SDM attenuator

The implemented two-tone generator has a frequency range of 15...180 kHz and achieves an SFDR of 60 dB with a word length of 15 bits, requiring a chip area of 0.02 mm<sup>2</sup>.

## III. RF SIGNAL GENERATION

Multi-tone RF stimuli are easily generated by combining the multi-tone generator from the last section with a digital sigma-delta modulation transmitter (Fig. 1). Due to the inherent low-pass characteristic of the PLL, no additional filter is needed to reconstruct the sine tones from the oversampled data stream.

The output frequency  $f_{out}$  of a fractional-N PLL with a reference frequency  $f_{ref}$  and a division ratio  $N = N_I + N_F$ , consisting of integer part  $N_I$  and fractional part  $N_F = FRAC/2^{wf}$ , is given by

$$f_{out} = f_{ref} \left( N_I + \frac{FRAC}{2^{wf}} \right) = N f_{ref} \quad (5)$$

where  $wf$  is the word length of the fractional accumulator and  $FRAC$  is the fractional word. The PLL is frequency-modulated in the digital domain by adding modulation data  $D(n)$  to the fractional word. The modulation data is low-pass filtered by the closed loop transfer function  $G(s)$  of the PLL [5]. A fast verification of  $|G(s)|$  can be performed by using the two-tone generator from section II and measuring the frequency response. Within the loop bandwidth,  $|G(s)| \approx 1$  and the digital data directly affects the PLL frequency:

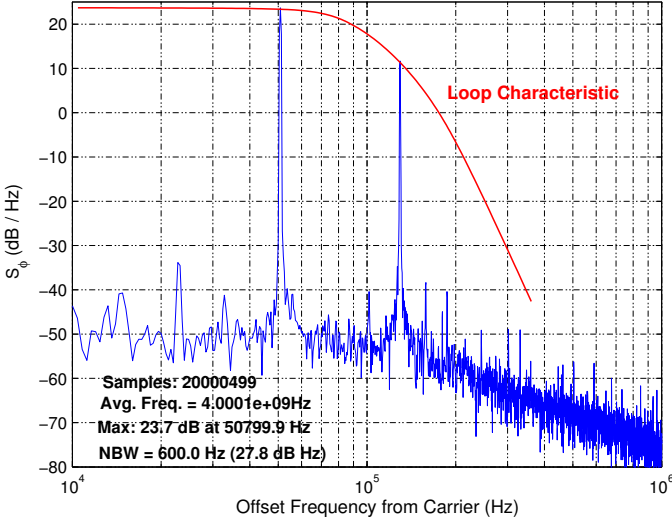


Fig. 4: Simulated two-tone spectrum at the PLL output

$$f_{out}(n) \approx f_{ref} \left( N_I + \frac{FRAC + D(n)}{2^{wf}} \right) = f_{ref} \left( N + \frac{D(n)}{2^{wf}} \right) \quad (6)$$

When  $D(n)$  is a digital sine wave with frequency  $f_{mod}$  and amplitude  $\hat{m} = \max[D(n)]$ , a peak PLL frequency deviation  $\widehat{\Delta f}$  is created of

$$\widehat{\Delta f} = \frac{\hat{m}}{2^{wf}} f_{ref} \quad (7)$$

for  $\hat{m} < 2^{wf}$ . This corresponds to a peak modulation index  $\hat{\mu}$  of

$$\hat{\mu} = \frac{\widehat{\Delta f}}{f_{mod}} = \frac{\hat{m}}{2^{wf}} \frac{f_{ref}}{f_{mod}} \quad (8)$$

With  $f_{ref} = 26$  MHz,  $f_{mod} = 100$  kHz,  $wf = 22$  and  $\hat{m} = 10916$  a GSM-like frequency deviation of  $\widehat{\Delta f} = 67.7$  kHz is achieved. The modulation index is  $\hat{\mu} = 0.68$ .

Fig. 4 shows a simulated two-tone signal at the output of a PLL with a loop bandwidth of 100 kHz. The low-pass characteristic of the PLL is marked by the bold line. The tone outside the loop bandwidth is attenuated by approx. 12 dB compared to the in-band tone which can be easily verified in a production test setup using conventional equipment or the built-in FM discriminator (section IV).

All simulations were performed with a standard VHDL simulator, using the methodology described in [6], [7]. The complete circuit in Fig. 1 including analog blocks like VCO and loop filter was modeled in VHDL, the simulated period data of the VCO and the filter response (section V) were dumped to a file and post-processed using Matlab.

#### IV. DIGITAL FM DISCRIMINATOR

On-chip analysis of the PLL transmit signal requires extracting and digitizing the RF phase / frequency information from the carrier which is a narrowband signal with large, constant amplitude. A standard RF receiver architecture is optimized for detecting low-level RF signals in the presence of strong interferers. It requires large area, precision analog circuitry like a mixer and a high resolution ADC. Instead, a much simpler demodulation technique is applied: a first order digital FM discriminator only consists of a high-speed dual-modulus divider and a D-flip-flop (Fig. 5) and delivers a sigma-delta modulated bit stream containing the demodulated data.

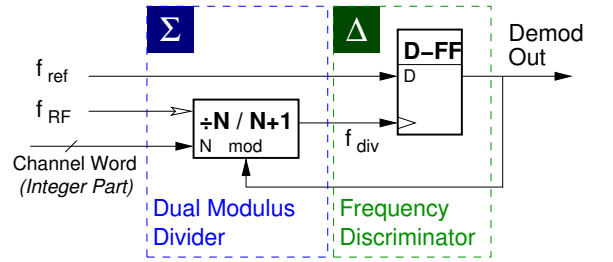


Fig. 5: First order sigma-delta frequency discriminator (SDFD)

The digital sigma-delta frequency discriminator and digitizer (SDFD) in [8] has been used for demodulating an FM IF signal. The proposed frequency discriminator takes advantage of the high transit frequency of the 130nm CMOS technology; it is directly clocked with the 4GHz signal of the VCO to create an even simpler RF BIST architecture.

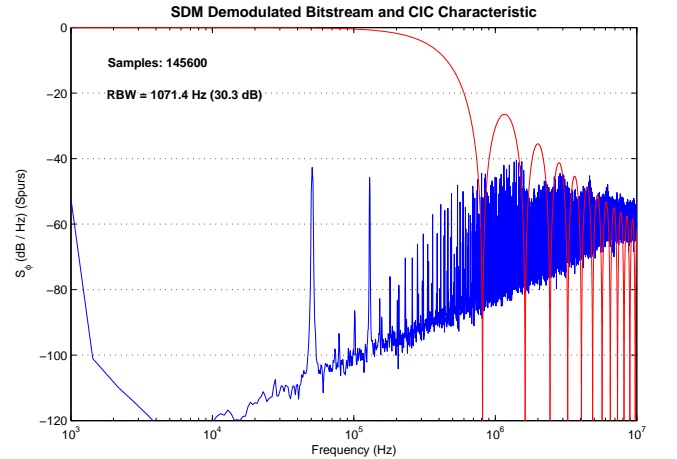


Fig. 6: Two-tone spectrum at SDFD output and transfer function of 2<sup>nd</sup> order CIC

The frequency deviation of the TX signal has to be limited to  $f_1 < f_{ref}/2$  to avoid aliasing, which is fulfilled automatically as the PLL bandwidth has to be much lower than  $f_{ref}$  for stability reasons. Just as the input signal of a sigma-delta ADC must not exceed the quantizer input step  $\pm q$  to avoid

an overload condition, the input frequency  $f_{RF}$  of the SDFD has to be within the limits

$$Nf_{ref} < f_{RF} < (N+1)f_{ref} \quad (9)$$

which is satisfied by using the channel word as the lower division ratio for the dual-modulus divider. Under these conditions, the demodulated output of the SDFD (Fig. 5) is an oversampled, first order sigma-delta modulated approximation of the frequency modulating signal as shown in Fig. 6.

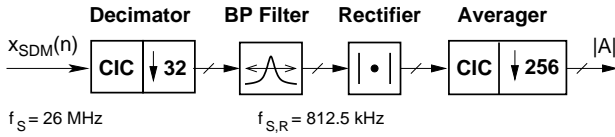


Fig. 7: Block diagram of amplitude estimator

The 20 dB/dec rise of the noise floor is due to the noise-shaping characteristic of the first order SDFD, the spurious tones at higher frequencies are still under analysis.

## V. DIGITAL NARROWBAND FILTERING

On-chip spectral analysis of the demodulated bit stream is a highly desirable feature because it eases the requirements on the production tester and enables device self-test in the final product. Instead of implementing a full-blown FFT, a narrowband frequency analysis is performed to estimate the amplitude only of certain frequency components. First, the SDM bit stream is decimated and pre-filtered with a cascaded integrator-comb (CIC) filter. The band of interest is then selected with a narrow, programmable LDI bandpass filter whose output is rectified and averaged in another CIC filter (Fig. 7).

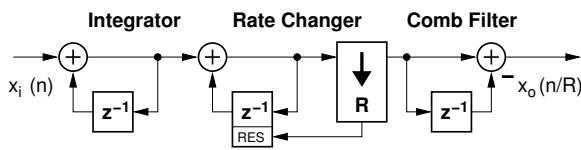


Fig. 8: Second order CIC filter with dump and reset

The first stage of this amplitude estimator is a second order CIC filter that decimates the SDM bit stream by a factor of  $R = 32$ . Its multiplier-less structure allows for a very compact implementation while running with the full sampling rate of  $f_s = 26$  MHz (Fig. 8) [9]. At least a second order CIC filter is required to suppress the high-frequency quantization noise components of the first order SDM bit stream with a maximum around  $f_s/2 = 13$  MHz. (10) predicts a worst case suppression of a second order ( $N = 2$ ) CIC with  $R = 32$  near  $f_s/2$  of 60 dB at 12.6 MHz ( $F = 15.5$ ) which is still sufficient to avoid excessive aliasing of quantization noise for this application.

$$\frac{|H(F)|}{|H(0)|} = \left| \frac{\sin \pi F}{\sin \frac{\pi F}{R}} \right|^N R^{-N} \approx |\text{sinc} \pi f|^N \text{ with } F \doteq \frac{fR}{f_s} \quad (10)$$

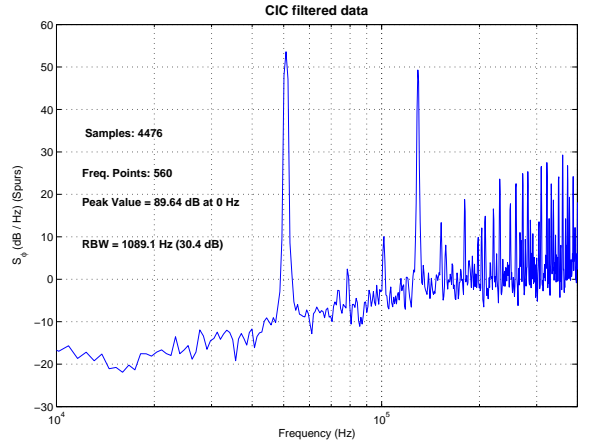


Fig. 9: Output spectrum of second order CIC decimator

The spectrum of the decimated two-tone signal is limited to  $f_s/32 = 812.5$  kHz (Fig. 9). Some quantization noise is folded back into the signal band, as can be seen near DC.

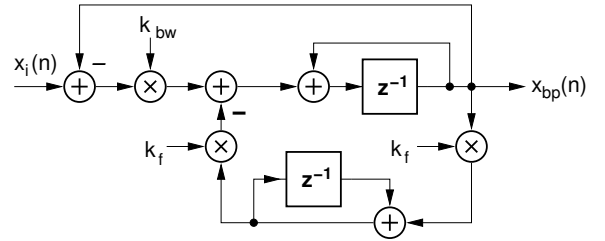


Fig. 10: Second order LDI BP filter

The narrow bandpass is implemented with a LDI structure similar to the multitone generator from section II with an additional damping term  $k_{BW}$  (Fig. 10) that determines the bandwidth. A main advantage of this filter type is its robustness against coefficient truncation:  $k_f$  is only 9 bits wide which gives a frequency resolution of 300 Hz without compromising noise performance. Another advantage is that the resonance frequency  $f_c$  is set with a single parameter  $k_f$  (11).

$$f_c = \frac{f_{S,R}}{\pi} \arcsin \frac{k_f}{2} \approx \frac{k_f f_{S,R}}{2\pi} \quad (11)$$

The reduced sampling rate of  $f_{S,R} = 812.5$  kHz allows the sharing of area expensive resources between blocks in the bandpass, here, a fourth order band-pass with parametrized center frequency is implemented with only one multiplier in an area of less than 0.03 mm<sup>2</sup>. Simultaneous multitone analysis could be performed at the cost of additional chip area by running several resonators in parallel [3].

Fig. 11 shows the simulation plot of the demodulated and bandpass-filtered signal of Fig. 4 with the bandpass centered at the second tone. The integrated spectrum indicates that the

suppression of the first tone and other disturbances is more than sufficient for a precise amplitude measurement.

## VI. CONCLUSIONS

In this paper, an area efficient method for a BIST of integrated RF transmitters, focused on spectral parameters has been presented. It relies entirely on digital components and has been implemented on a 130nm CMOS test chip in an area of only 0.05 mm<sup>2</sup>. Measurement data will be available in summer. Multi-tone stimuli with a SFDR of 60 dB are generated utilizing a robust LDI oscillator and upconverted using the sigma-delta modulation transmit PLL. The FM modulated RF signal is downconverted and digitized with a digital FM discriminator, achieving a SNR of 80 dBc. Spectral performance is measured on-chip using a compact, narrowband LDI bandpass. The implemented BIST architecture does not interfere with critical RF signal paths as the signal generation and demodulation is performed entirely in the digital domain, making it well suited for highly integrated RF CMOS circuits.

## ACKNOWLEDGMENT

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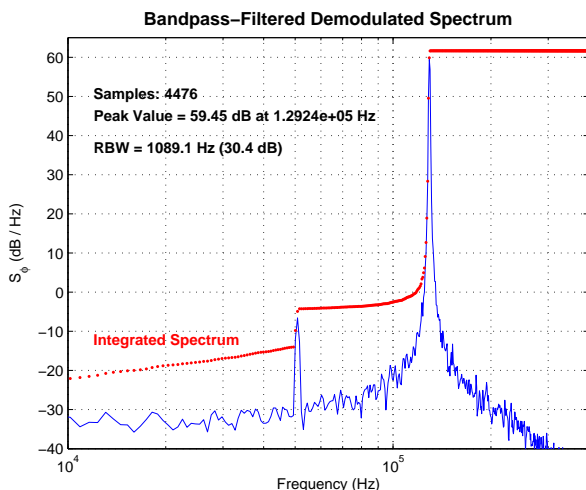


Fig. 11: Demodulated and bandpass-filtered two-tone spectrum