

Digital RF CMOS Transceivers for GPRS and EDGE

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Abstract — A GPRS RF solution using sigma-delta modulation and an EDGE RF solution using digital polar modulation are presented. The single-chip, quad-band transceivers have been implemented in a 0.13 μm CMOS technology. The lock-in time of the sigma-delta modulator with integrated loop filter is less than 120 μs with a phase error of 1.2° rms and an output power of 3.5 dBm; it is fully compliant to the GSM specification. The EDGE transceiver shows a nominal margin of 11 dB to the critical 400 kHz specification with a transmit EVM of 2.5%.

Index Terms — CMOS, EDGE, GPRS, transceiver, polar modulator, sigma-delta modulator.

I. INTRODUCTION: TECHNOLOGY & SYSTEM TRENDS

Advanced bipolar and compound semiconductor technologies still offer advantages for ultra high frequencies and special applications (PA's, automotive radar). But the superior integration densities of pure CMOS technologies and the lower costs make them better suited for consumer markets with their continuous pressure for more functionality and lowest bill-of-material (BOM).

New transceiver architectures incorporating digital signal processing compensate for the weaknesses of CMOS technologies like flicker noise and wider parameter spread and make CMOS the technology of choice for low-cost, high performance cellular transceivers.

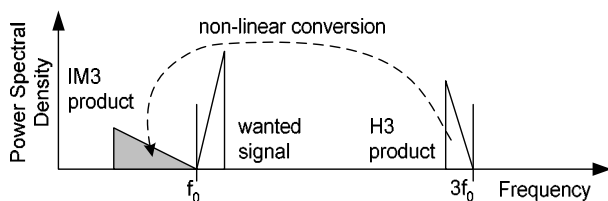


Fig. 1 VCO distortion by PA feedback

Nowadays, the receive path of most integrated GPRS / EDGE transceiver circuits is implemented as a direct conversion architecture, although it took several years to solve the problems of flicker noise and DC offset in mass production. Its low power consumption, low BOM and good image rejection without external filters are important advantages over heterodyne architectures.

The focus of this paper is on the different architectural options for the transmit path: Section II describes the design trade-offs of direct modulation (DM), section III shows a single-chip CMOS GPRS transceiver based on sigma-delta modulation (SD) and Section IV presents an EDGE transceiver utilizing a digital polar modulator (PM).

II. DIRECT MODULATION ARCHITECTURE

At present, most commercially available GPRS / EDGE transceivers are based on direct conversion architectures. Although the principle of a direct modulation transmitter looks simple, one of the main design challenges is feedback from the PA (modulated) to the VCO (unmodulated) [1], causing spurious sidebands.

Running the VCO at a largely different frequency than the output frequency alleviates this problem which is usually achieved by an offset PLL or by frequency division of the VCO [2]. The latter doesn't require an additional oscillator and mixer but is still sensitive to harmonics of the PA, especially to those of the 3rd order (H3) (Fig. 1). This means that external filtering of the transmit signal is required on the board level in addition to a shielding box for the RF chip.

As a reference, a quad-band GPRS / EDGE transceiver chip implemented in a 0.25 μm BiCMOS technology is presented that was targeted for high-end mobile phones [3]. It consists of a direct conversion architecture for both receive and transmit path in a mainly analog implementation. LO generation is performed using a single core RF VCO with digital pre-tuning and a low-modulus fractional-N synthesizer. An on-chip voltage controlled crystal oscillator (VCXO) generates the reference frequency which is fine-tuned by a DAC on the base-band processor.

The receive path features a mixer with DC offset compensation and a programmable gain amplifier (PGA). With this architecture, a baseband ADC with a resolution of 10 to 12 bit is sufficient.

For the transmit path, an external variable gain amplifier, a H3 filter and a shielding box are needed to achieve the dynamic range and spectral purity required for the EDGE

standard. In spite of these drawbacks, direct conversion can be the optimum architecture for a BiCMOS technology with a relatively low digital complexity or for higher modulation bandwidth requirements as in CDMA or UMTS.

III. SIGMA-DELTA MODULATION ARCHITECTURE

One of the main challenges of designing RF transceivers in a standard CMOS technology is the larger parameter spread compared to technologies optimized for analog performance. One of the advantages of standard CMOS technologies is the high integration level for digital logic which enables the use of advanced DSP techniques for on-chip calibration loops and signal correction. As a result, the optimum architecture of an RF CMOS transceiver is different from a BiCMOS solution.

A quad-band GSM transceiver implemented in a 0.13 μm CMOS technology with a digital sigma-delta modulation transmitter is presented in Fig. 2 [4]. The integrated VCO runs at a multiple of the *modulated* transmit frequency, therefore it is much less sensitive to PA feedback than a direct conversion architecture. Targeted at the mass market, the transmitter requires no cost-intensive shielding box or external filters but is limited to constant envelope modulation. Due to the high reference frequency of the $\Sigma\Delta$ fractional-N synthesizer, the size of the loop filter capacitors is reduced drastically, allowing on-chip integration. In order to compensate for tolerances of on-chip components, a digital loop filter calibration is implemented. Despite all digital calibrations, an excellent overall settling time of less than 120 μs is achieved.

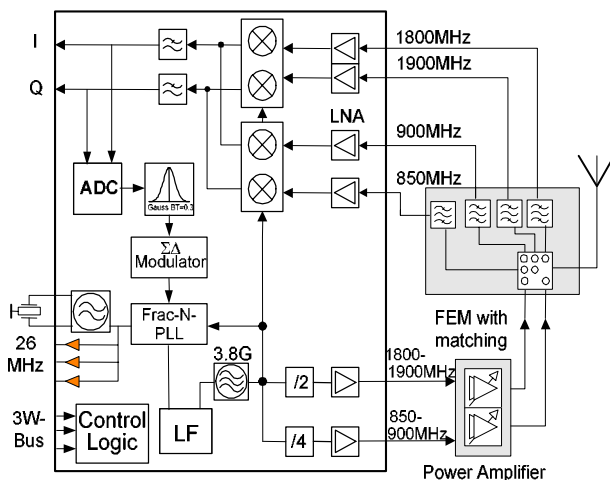


Fig. 2 GPRS transceiver with sigma-delta modulator

The H3 problem of direct modulation is avoided by modulating the VCO frequency in a digital way: In order to achieve a signal bandwidth exceeding the closed loop bandwidth of the PLL, the modulator architecture depicted in Fig. 3 uses digital filtering plus pre-emphasis. The DigRF digital baseband interface standard [5] is enabled by the digital filtering within the RF transmitter, eliminating the transmit DAC on the baseband processor.

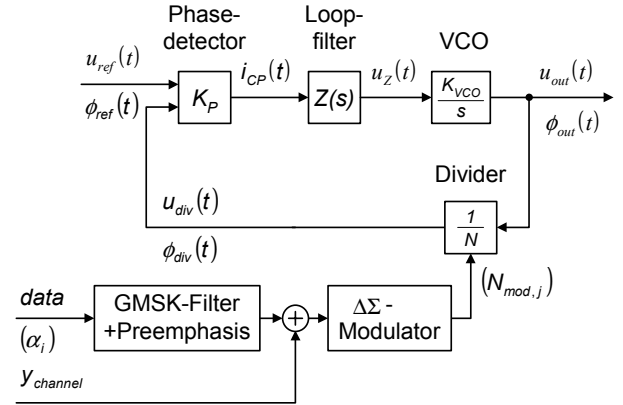


Fig. 3 Fractional-N modulator using pre-emphasis

The pre-emphasis filter requires a transfer characteristic equal to the inverse of the closed-loop transfer function $G(s)$. A similar technique is presented in [6]. The transfer function derived from Fig. 3 is given by

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = N \cdot \frac{1}{1 + \frac{N}{K_p K_{VCO}} \frac{s}{Z(s)}} = N \cdot G(s) \quad (1)$$

where N is the divider value, K_p [A/rad] and K_{VCO} [rad/Vs] are the conversion gain values for the phase-detector and the VCO respectively. $Z(s)$ [Ω] is the Laplace transformation of the loop filter transimpedance.

The output frequency of the VCO $f_{out}(s)$ of the fractional-N frequency synthesizer is given by

$$f_{out}(s) = N_{mod}(s) \cdot f_{ref} \cdot G(s) \quad (2)$$

where $N_{mod}(s)$ is the according representation in the complex frequency domain. When the modulation data is filtered by the inverse of the closed-loop transfer function $G(s)$ the output frequency of the VCO can be derived as

$$f_{out}(s) = N_{mod}(s) \cdot f_{ref} \cdot G(s) \cdot G(s)^{-1} = N_{mod}(s) \cdot f_{ref} \quad (3)$$

A constant open loop gain is achieved by a digital adjustment algorithm OLGA² (Open Loop Gain Auto Adjustment) which compensates parameter variations.

signal processing as possible. A very good control of analog mismatches is achieved by a combination of compensation algorithms for amplitude and phase part, similar to the algorithm described in section III. One of the most critical parameters of mismatch is the time delay between amplitude and phase signal.

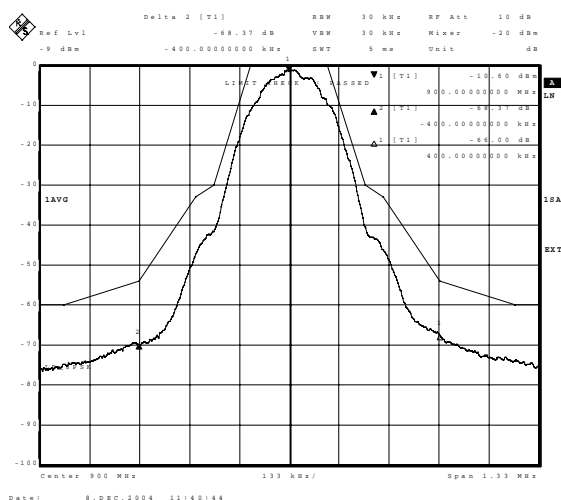


Fig. 8 Measured EDGE spectrum

Table I shows the degradation of spectral emissions and modulation accuracy as a function of AM / PM delay mismatch. Although modulation accuracy (defined by EVM) is also affected by amplitude-phase-delay, table I shows that the spectrum mask is the more stringent specification for AM / PM delay mismatch. A delay mismatch of less than 4/96 symbol times (~0.15 μ s) is required to keep spectral emissions below -54 dBc at the 400 kHz corner as required by the EDGE specifications. At this mismatch, RMS EVM is still well below the specification limit of 9%.

TABLE I
INFLUENCE OF AMPLITUDE-PHASE-DELAY ON EDGE SPECTRUM

Delay Mismatch $\times/96 * T_{sym}$	EVM RMS %	Spectrum @ 400 kHz dBc
0	0.0	-72.5
1	0.4	-62.5
2	0.7	-57.6
3	1.1	-54.5
4	1.5	-52.2

These values show that good knowledge and control of AM and PM delays are essential. The high amount of digital signal processing of the presented polar modulation

transmitter makes it a lot easier to predict the delays in both paths, compared to an analog implementation. In addition, the highly digital architecture is more robust to environmental or process variations, thus preserving the spectral purity and modulation accuracy. Fig. 8 shows a measured output spectrum, in comparison to the EDGE mask, demonstrating large margins at the critical 400 kHz corner.

V. CONCLUSION

This presentation has shown the architectural evolution of GPRS / EDGE transceivers required by migrating from BiCMOS to CMOS technologies. Digital algorithms and calibration loops compensate for environmental and process variations, resulting in robust RF CMOS transceivers.

TABLE II
OVERVIEW OF TRANSMIT ARCHITECTURES

	DM	SD	PM	PT
EDGE	yes	no	yes	yes
Preferred Technology	BiCMOS	CMOS	CMOS	CMOS
Lin. PA?	yes	no	yes	no
BOM	high	low	medium	low

VI. ACKNOWLEDGEMENT

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