A Compact Multi-Tone Test Generator for RF ICs

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Motivation for Test Improvements in RF Transceivers

Growing contribution of test costs to production costs!!!

Reasons

- SOC: more system tests have to be performed by chip maker
- Slow and expensive RF – tests
- Falling production costs (smaller chips) but constant tester costs
## Critical Production tests for RF Transmitters

<table>
<thead>
<tr>
<th>Test</th>
<th>Challenge</th>
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<tbody>
<tr>
<td><strong>Modulation Spectrum (Mask Conformity)</strong></td>
<td>- Long averaging times</td>
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<tr>
<td></td>
<td>- Complex signal analysis</td>
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<tr>
<td><strong>Out-of-Band Spectrum (Phase Noise, Spurs)</strong></td>
<td>- Long averaging times</td>
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<td></td>
<td>- Complex signal analysis</td>
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<tr>
<td></td>
<td>- Dynamic range</td>
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<tr>
<td><strong>PLL Loop Bandwidth</strong></td>
<td>- Difficult to measure directly</td>
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<tr>
<td><strong>VCO / Divider Functionality</strong></td>
<td>- No direct access to supply voltages</td>
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<td>(integrated regulator) and LO signal</td>
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<td></td>
<td>- Lots of failure modes</td>
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<tr>
<td></td>
<td>(multiple VCO – Bands and division ratios)</td>
</tr>
<tr>
<td><strong>Output Power</strong></td>
<td>- Matching Chip – Board – Tester</td>
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</tbody>
</table>
Targets for RF IC BIST / BISC

- Get rid of expensive and slow RF test equipment
- Do not interfere with critical RF paths on-chip
- Generate little area overhead
- Do not generate additional failure modes in test circuitry, make test circuitry testable
- Modern CMOS technologies (130nm → 65 nm) favor digital over analog implementations

Mainly digital implementation!

BIST: Built-In Self Test
BISC: Built-In Self Calibration
Built-In Self Test Concept for RF Transceivers
Test Signal Generation Using Sigma-Delta PLL

Reference Frequency

PFD

Loop Filter

VCO

\( \div N / N+1 \)

dig

TX Filter

0

1

Data

TE_1

Pattern Generator

dig

Dig. Multitone Generator

TE_2

Carrier Freq. Word

d_q(n)

additional BIST block

TE: Test Enable
Simple Pattern Generator Using LFSR

PRBS generator with a sequence length of $2^9-1$ made from a 9 Bit LFSR:

Can be easily configured for generation of short deterministic sequences like 01, 0001 as well!

**LFSR**: Linear_Feedback Shift Register

**PRBS**: Pseudo-Random Binary Sequence
Outline

- Motivation
- BIST Concept for RF Transceivers
- Test-Tone Generator
- Simulation Results
Lossless Digital Integrator Oscillator

- 2 N x N Multipliers
- 2 N-Bit Accumulators
Replace Multiplier by Sigma-Delta Attenuator

PLL has low-pass characteristic – no additional low-pass filter (LPF) needed in our case!
Replace N x 1 Bit Multiplier by Multiplexor

_\textit{N x 1 Bit Multiplier}_

\[ x(n+1) \rightarrow \text{SDM} \rightarrow \times \rightarrow \text{LPF} \rightarrow bx(n) \]

\[ x(n+1) \rightarrow \text{SDM} \rightarrow \times \rightarrow \text{LPF} \rightarrow bx(n) \]

_\textit{N Bit 2:1 Multiplexor}_

\[ 0 \rightarrow x(n) \rightarrow 1 \]

\[ \text{Select } bx(n) \text{ based on } b \]
Digital Tone Generator Using SDM Attenuator

- 1 Bit Shifter (fixed)
- 4 N Bit Accumulators
- 2 N-Bit Adders
- 1 N-Bit 2:1 Multiplexor
Use time-division multiplexing to share hardware for several tones

- 4 extra N-Bit registers needed per tone
Outline

- Motivation
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- Test-Tone Generator
- Simulation Results
Two-Tone Spectrum of Digital Sine Generator (Parallel Out)

\[
N = 15
\]

PSD of MUSIG Output

\[
a_1 = 2^4
\]

\[
b_1 = 0.012634 \Rightarrow f_1 = 55.9 \text{ kHz}
\]

\[
b_2 = 0.12201 \Rightarrow f_2 = 173.7 \text{ kHz}
\]

SFDR: ca. 60 dB

\[
S_V (\text{dB/Hz, Spur})
\]

Frequency (Hz)

\[
10^1 \quad 10^5 \quad 10^5
\]
Two-tone Spectrum of Digital Sine Generator (SDM Out)

$N = 15$

PSD of SDM Attenuator Output

$a_1 = 2^4$

$b_1 = 0.012634 \Rightarrow f_1 = 55.9 \text{ kHz}$

$b_2 = 0.12201 \Rightarrow f_2 = 173.7 \text{ kHz}$

SFDR: ca. 60 dB

-40 dB/dec

$S_v \text{ (dB/Hz, Square)}$

$10^4$ $10^5$ $10^6$ $10^7$

Frequency (Hz)
Two-Tone Spectrum at PLL Output

VCO Power Spectral Density

- $S_o$ (dB/Hz)
- Offset Frequency from Carrier (Hz)
- Loop Characteristic ($f_{3dB} = 100$ kHz)

- $a = 2^4$
- $b_1 = 0.012634 \Rightarrow f_1 = 55.9$ kHz
- $b_2 = 0.12201 \Rightarrow f_2 = 173.7$ kHz

Measure Loop Characteristics Using Two-Tone Signal
Results

- A completely digital two-tone test oscillator was implemented in a 130 nm CMOS process
- The oscillator allows measurement of PLL loop characteristic and marker generation
- Additional area for
  \( N=15 \) Bit, \( f_S = 26 \) MHz, \( f_{OUT} = 30 \ldots 300 \) kHz:
  - 1 Tone Generator \( A = 0.01 \) mm\(^2\)
  - 2 Tone Generator \( A = 0.015 \) mm\(^2\)
Thank You for Your Attention!