

Infineon

A Compact Multi-Tone Test Generator for RF ICs

Analog Workshop 2005 TU München

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Outline

Motivation

BIST Concept for RF Transceivers

Test-Tone Generator

Simulation Results

Motivation for Test Improvements in RF Tranceivers

Growing contribution of test costs to production costs!!!

Reasons

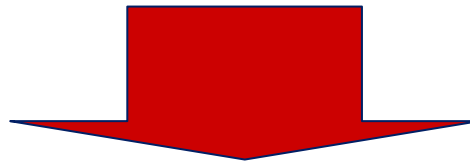
- **SOC: more system tests have to be performed by chip maker**
- **Slow and expensive RF – tests**
- **Falling production costs (smaller chips) but constant tester costs**

Critical Production tests for RF Transmitters

Test	Challenge
Modulation Spectrum (Mask Conformity)	<ul style="list-style-type: none"> - Long averaging times - Complex signal analysis
Out-of-Band Spectrum (Phase Noise, Spurs)	<ul style="list-style-type: none"> - Long averaging times - Complex signal analysis - Dynamic range
PLL Loop Bandwidth	<ul style="list-style-type: none"> - Difficult to measure directly
VCO / Divider Functionality	<ul style="list-style-type: none"> - No direct access to supply voltages (integrated regulator) and LO signal - Lots of failure modes (multiple VCO – Bands and division ratios)
Output Power	<ul style="list-style-type: none"> - Matching Chip – Board – Tester

Targets for RF IC BIST / BISC

- Get rid of expensive and slow RF test equipment
- Do not interfere with critical RF paths on-chip
- Generate little area overhead
- Do not generate additional failure modes in test circuitry, make test circuitry testable
- Modern CMOS technologies (130nm → 65 nm) favor digital over analog implementations



Mainly digital implementation!

BIST: Built-In Self Test
BISC: Built-In Self Calibration

Outline

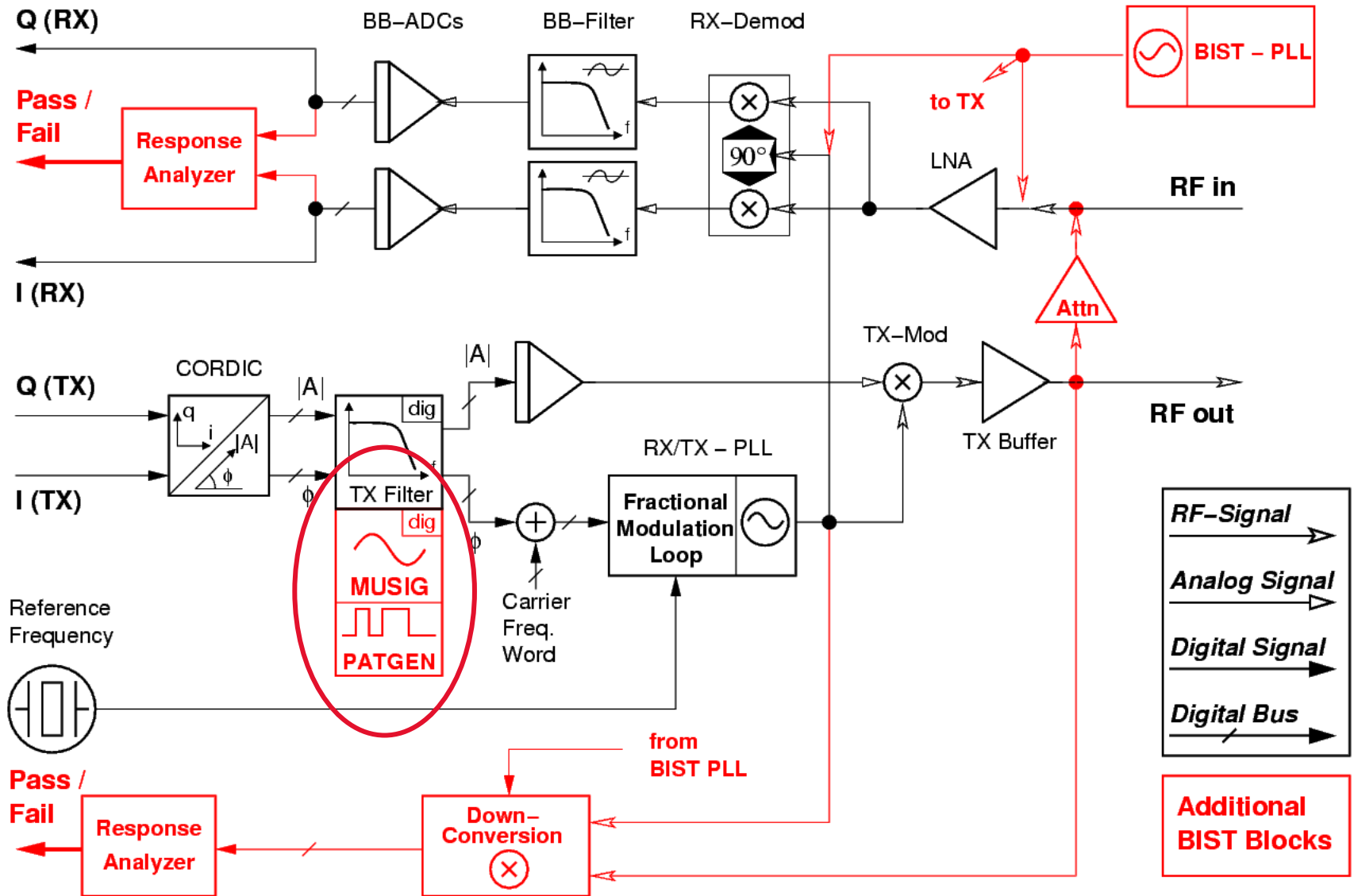
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Built-In Self Test Concept for RF Transceivers

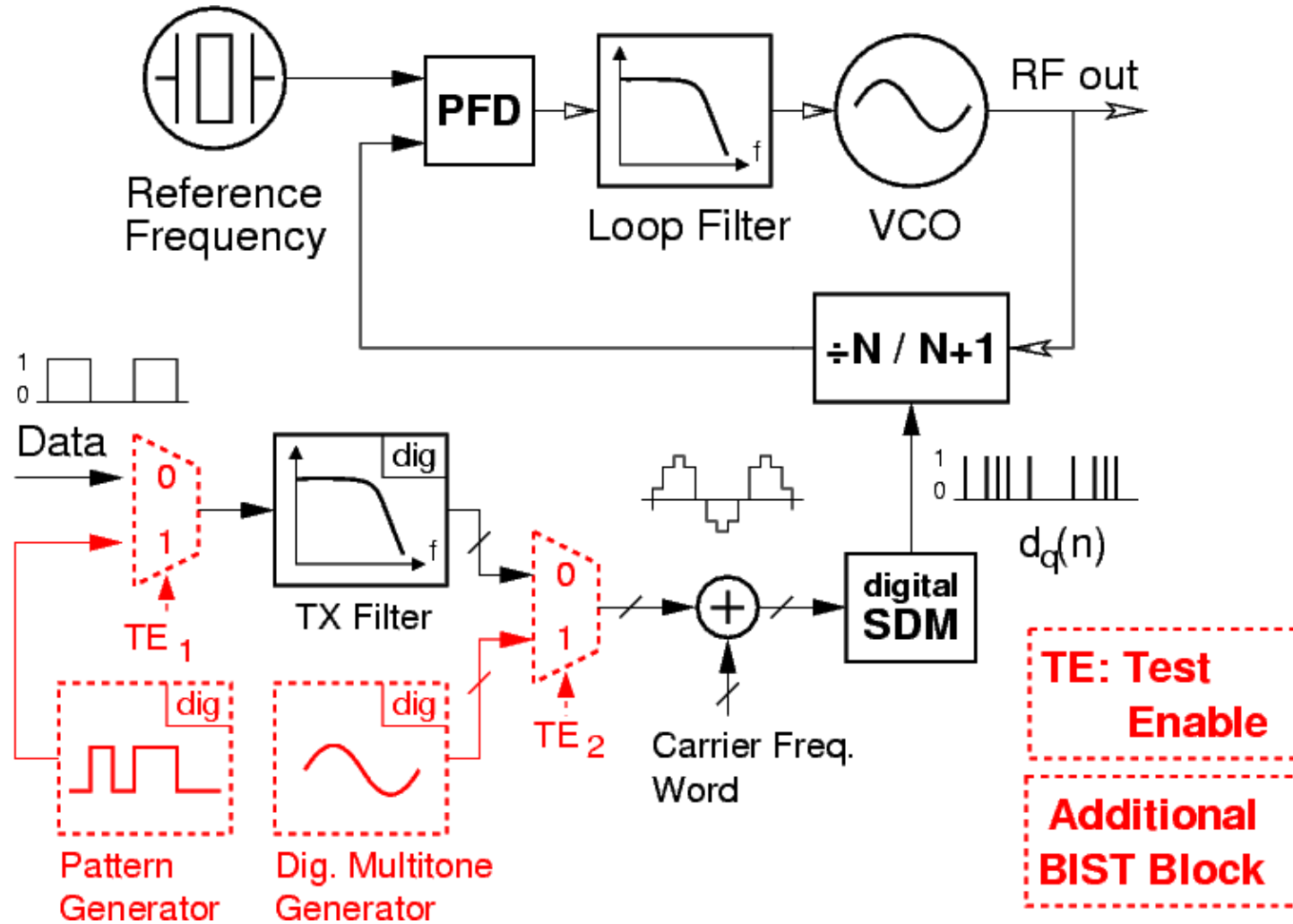


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Test Signal Generation Using Sigma-Delta PLL



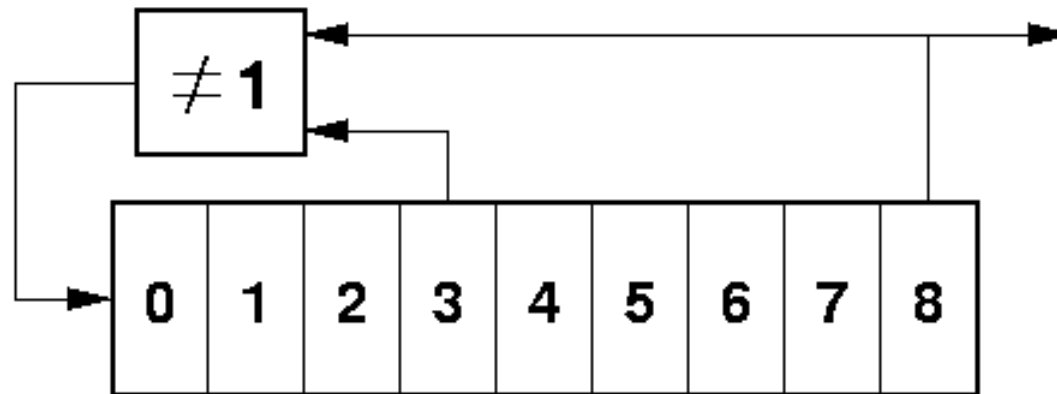
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Simple Pattern Generator Using LFSR

PRBS generator with a sequence length of 2^9-1
made from a 9 Bit LFSR:



Can be easily configured for generation of short deterministic sequences like 01, 0001 as well!

LFSR: Linear_Feedback Shift Register
PRBS: Pseudo-Random Binary Sequence

Outline

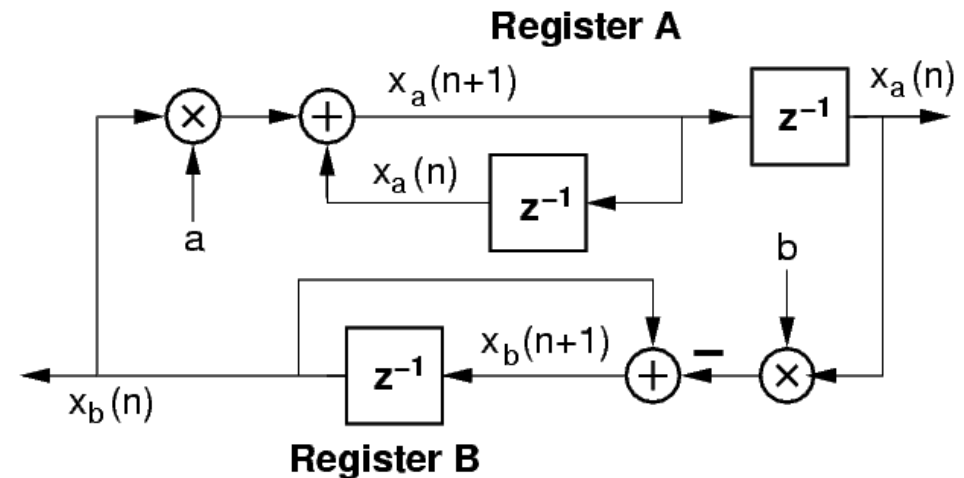
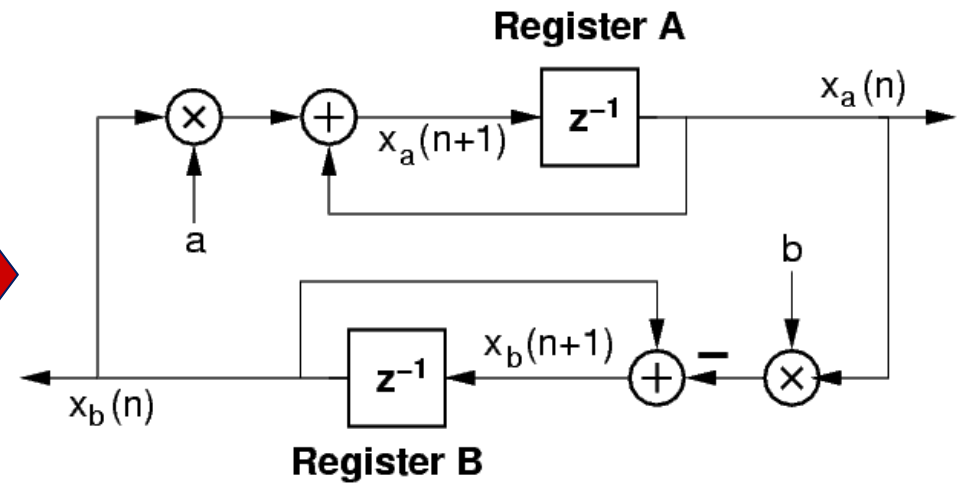
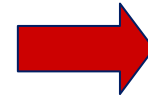
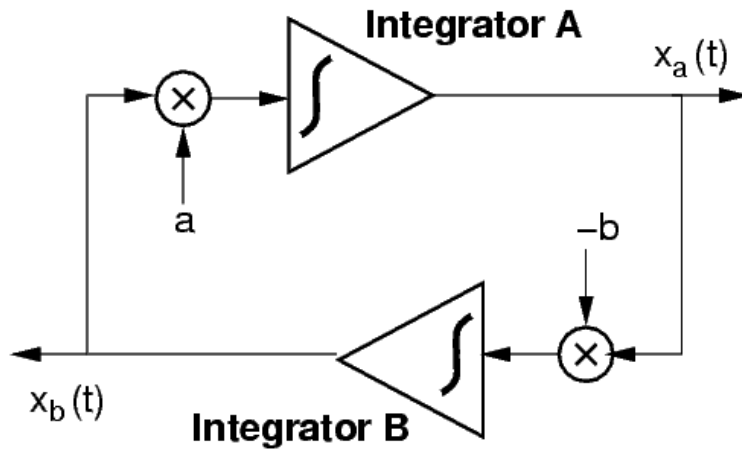
■ Motivation

■ BIST Concept for RF Transceivers

■ **Test-Tone Generator**

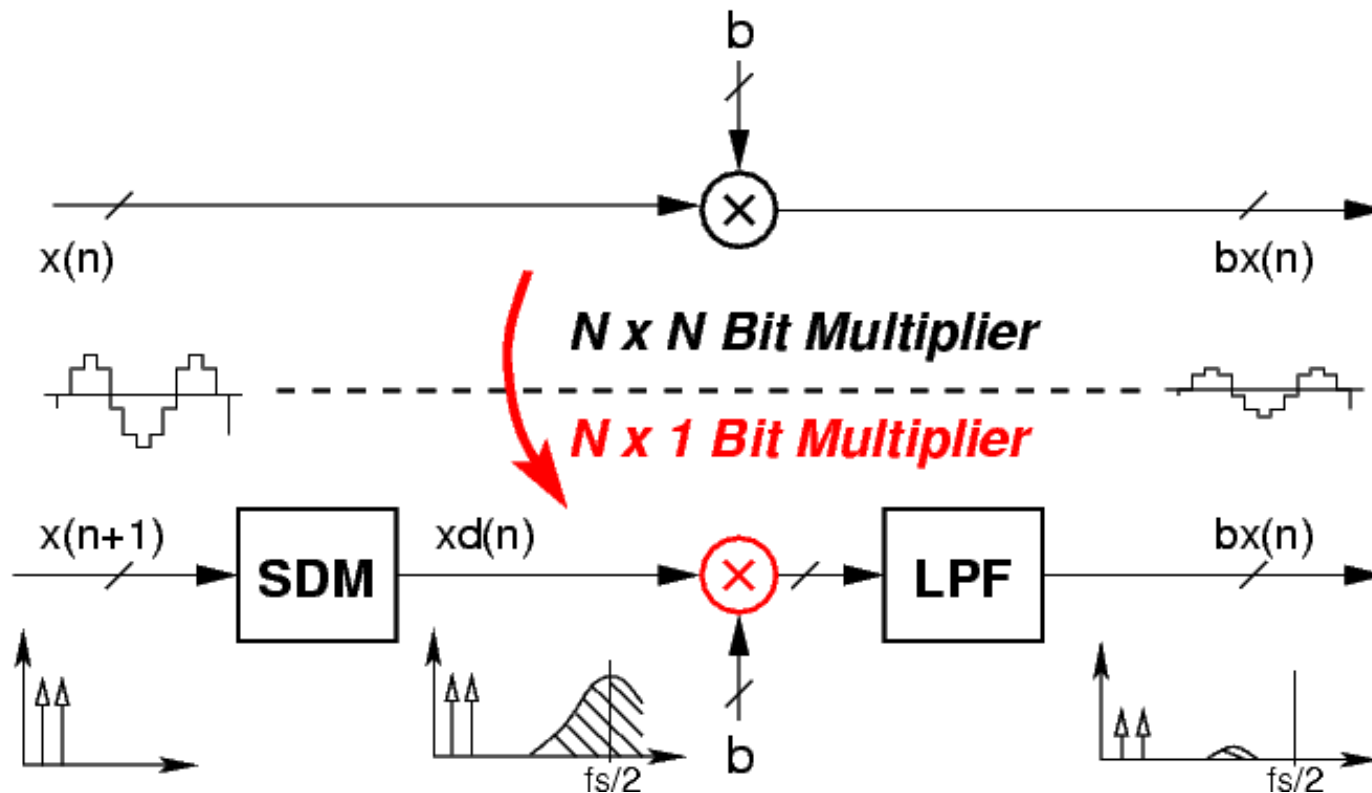
■ Simulation Results

Lossless Digital Integrator Oscillator



- 2 N x N Multipliers
- 2 N-Bit Accumulators

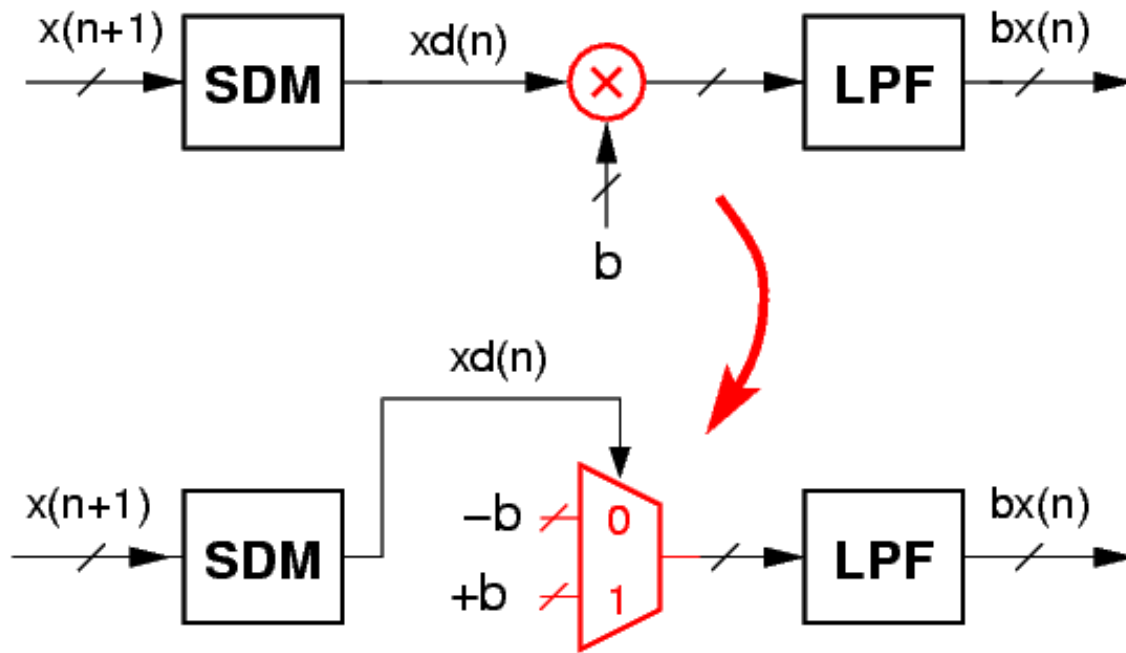
Replace Multiplier by Sigma-Delta Attenuator



PLL has low-pass characteristic – no additional low-pass filter (LPF) needed in our case!

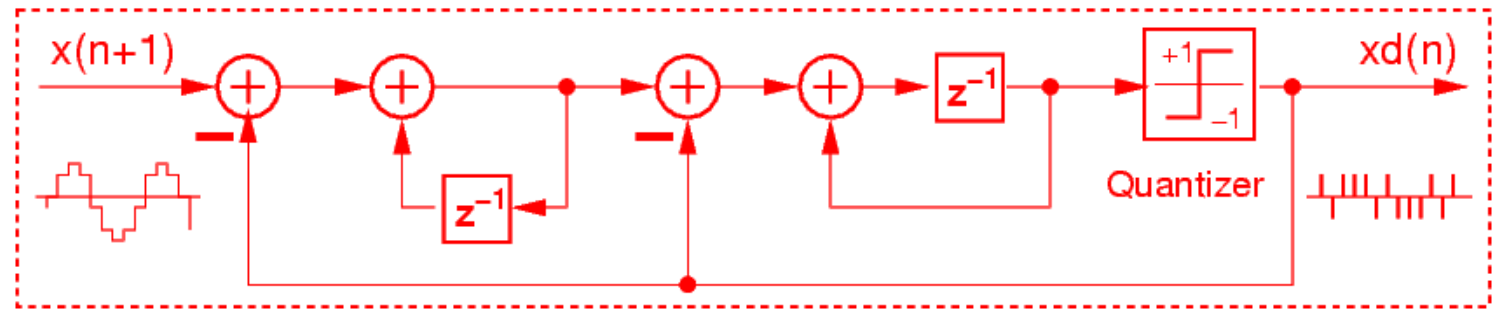
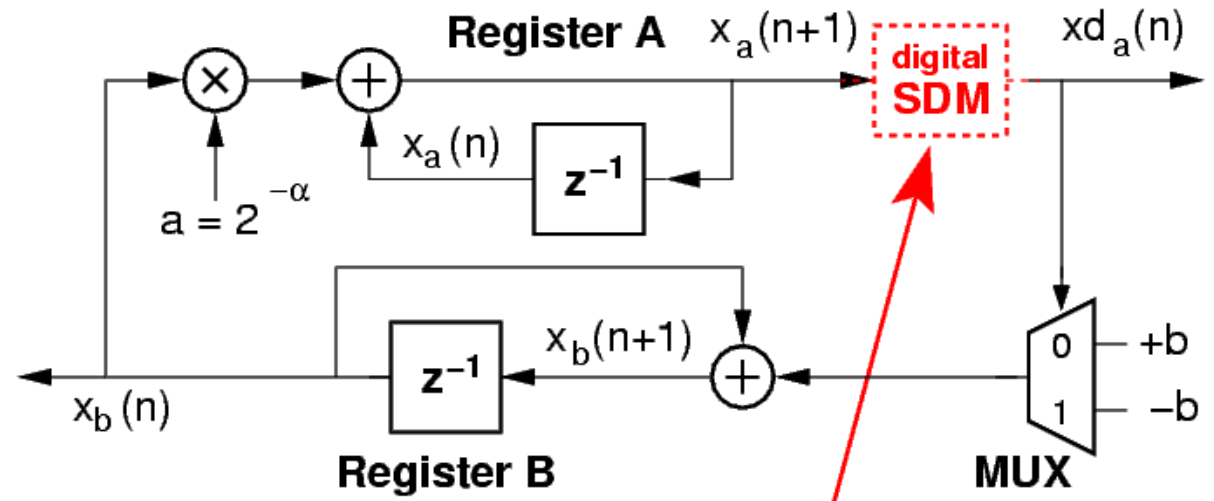
Replace N x 1 Bit Multiplier by Multiplexor

N x 1 Bit Multiplier



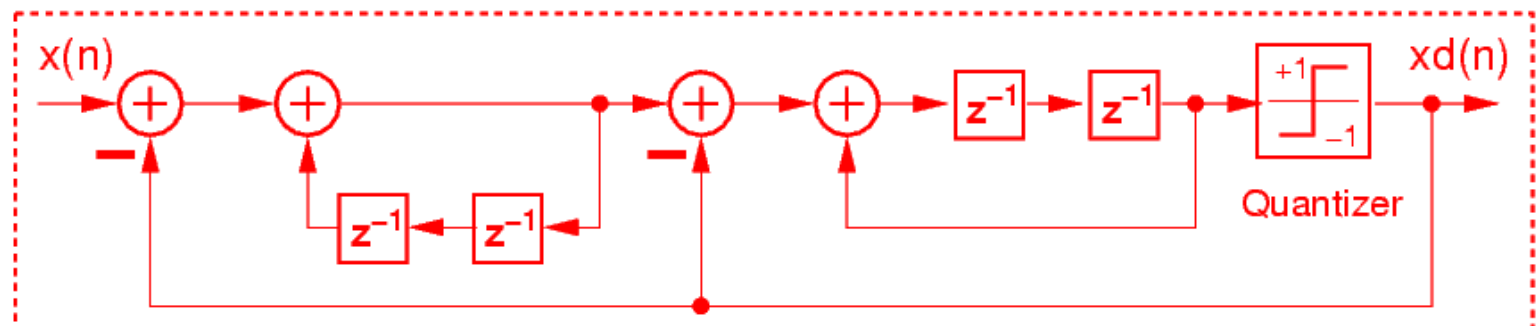
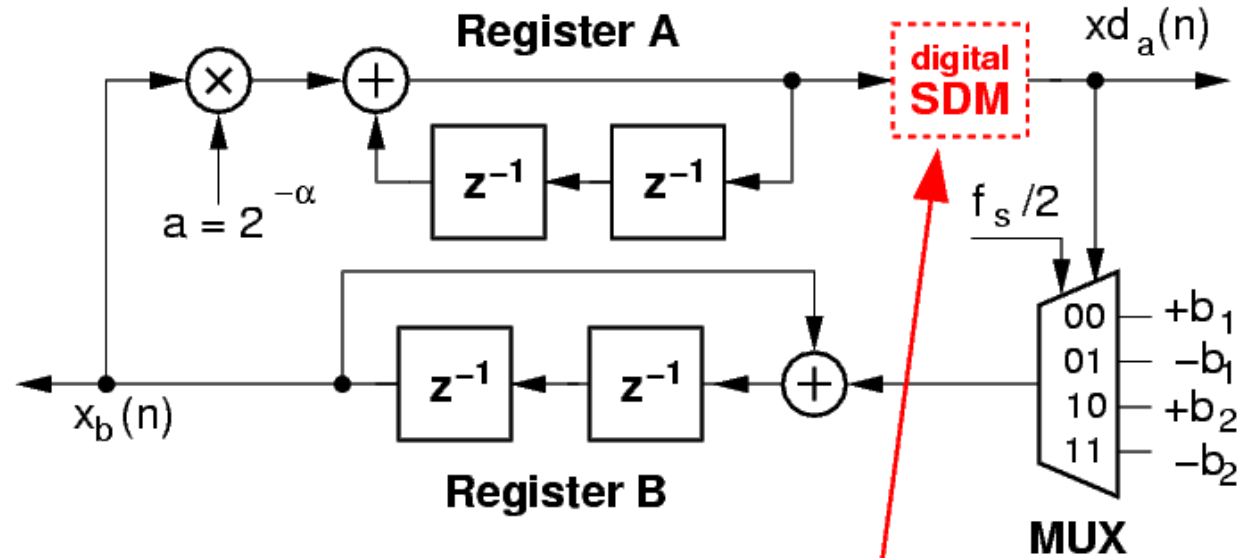
N Bit 2:1 Multiplexor

Digital Tone Generator Using SDM Attenuator



- 1 Bit Shifter (fixed)
- 2 N-Bit Adders
- 4 N Bit Accumulators
- 1 N-Bit 2:1 Multiplexor

Digital Multi-Tone Generator Using SDM Attenuator



- Use time-division multiplexing to share hardware for several tones
- 4 extra N-Bit registers needed per tone

Outline

■ Motivation

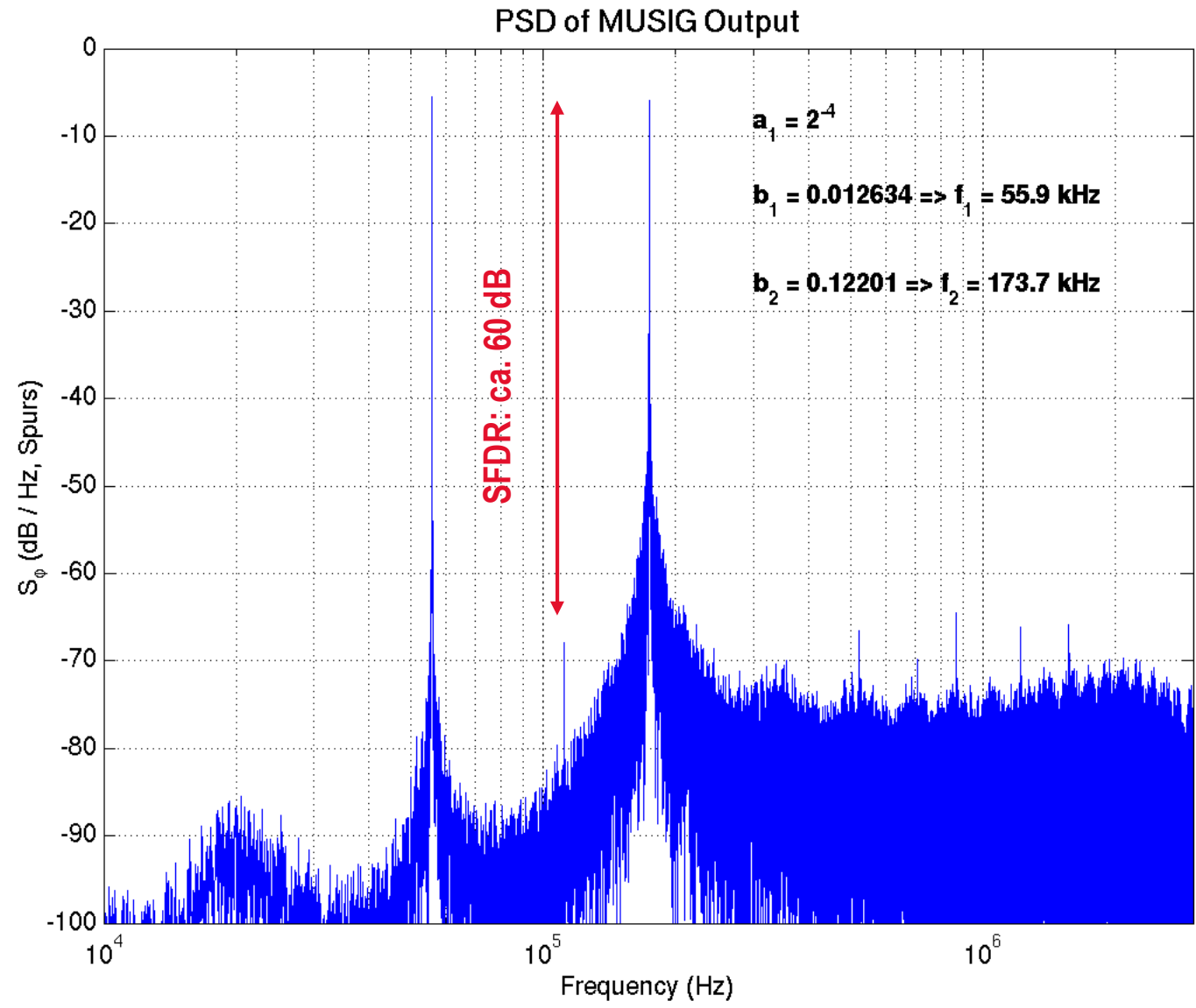
■ BIST Concept for RF Transceivers

■ Test-Tone Generator

■ **Simulation Results**

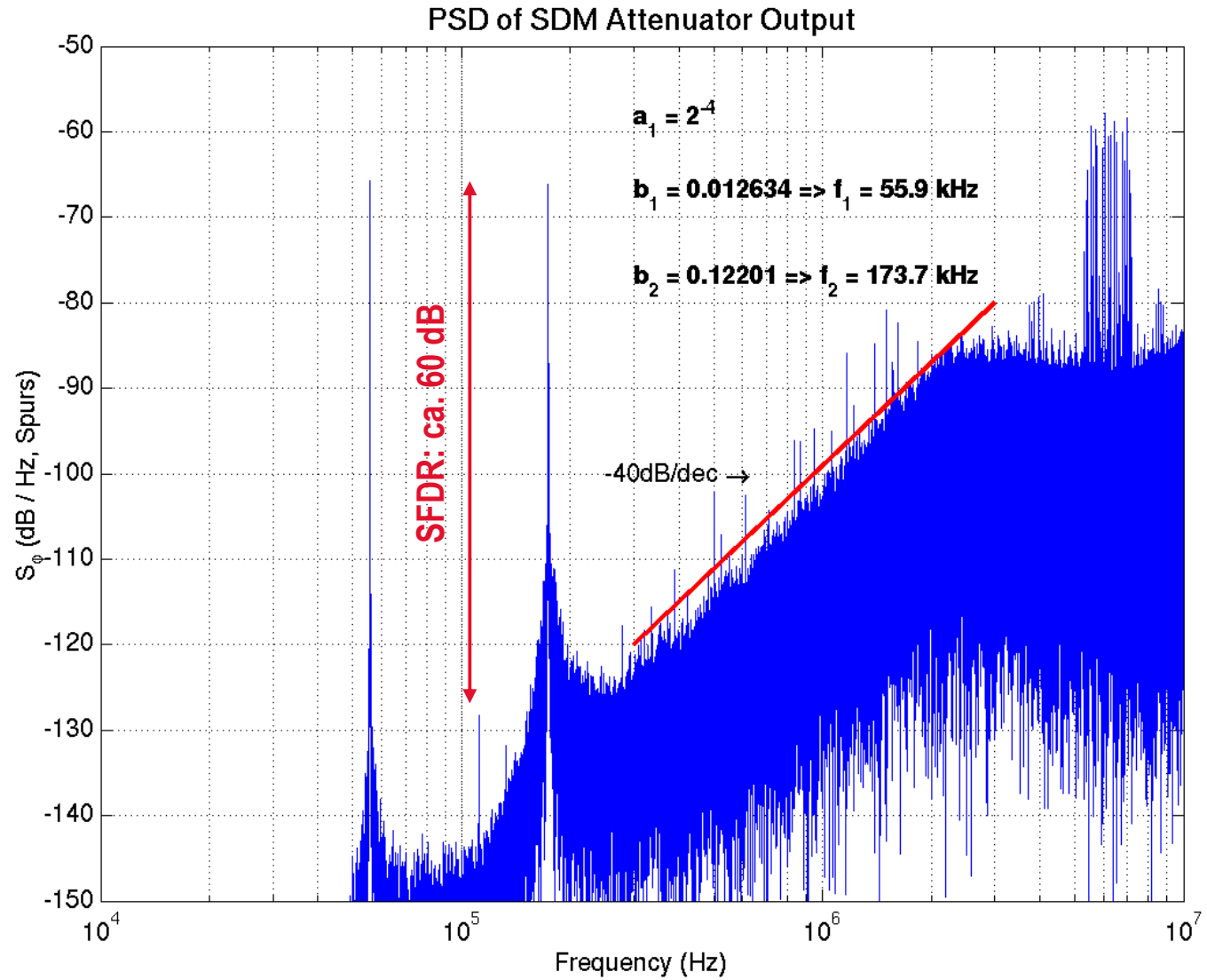
Two-Tone Spectrum of Digital Sine Generator (Parallel Out)

N = 15

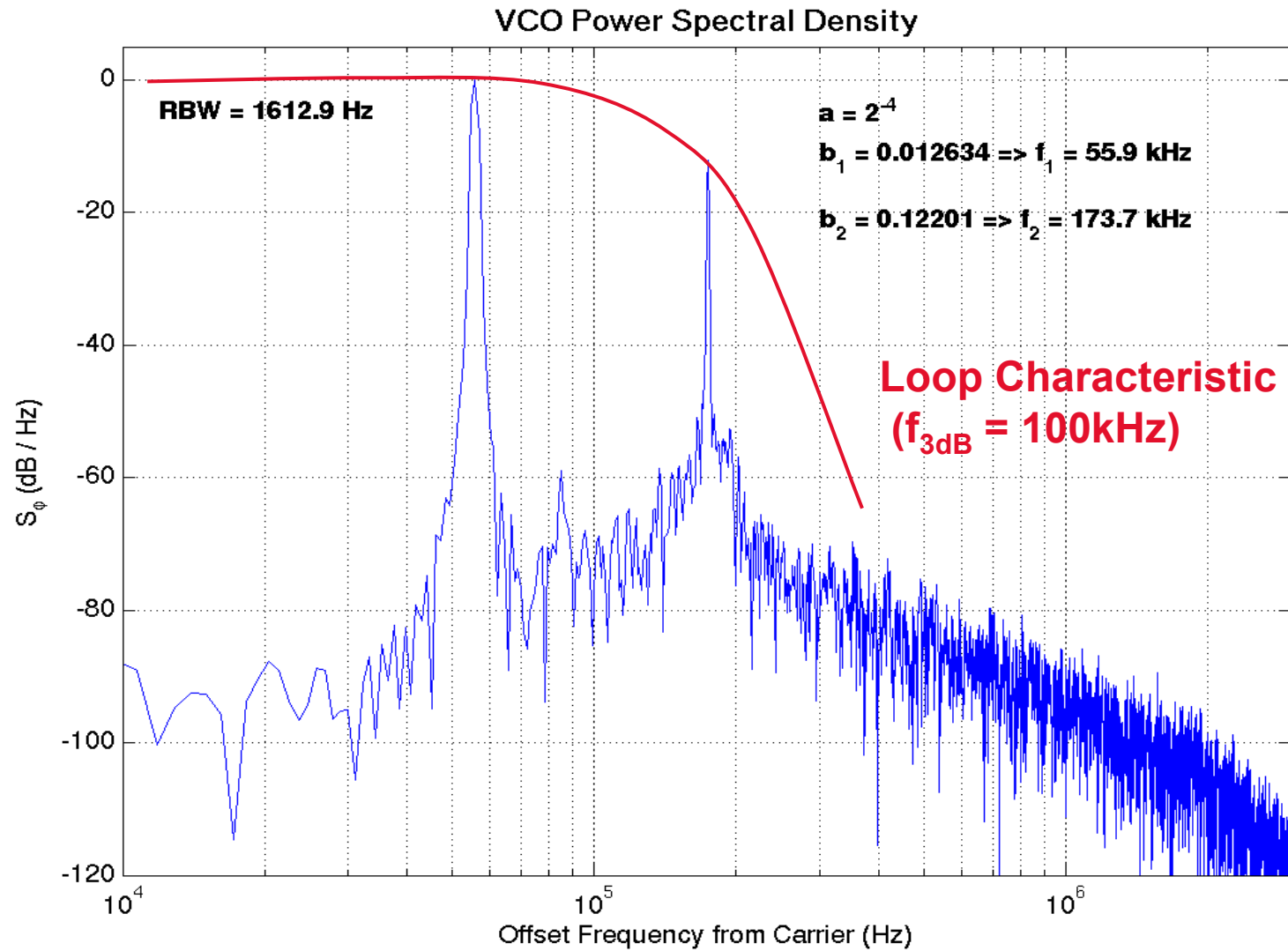


Two-tone Spectrum of Digital Sine Generator (SDM Out)

N = 15



Two-Tone Spectrum at PLL Output



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■ Measure Loop Characteristics Using Two-Tone Signal

Results

- A completely digital two-tone test oscillator was implemented in a 130 nm CMOS process
- The oscillator allows measurement of PLL loop characteristic and marker generation
- Additional area for
N=15 Bit, $f_S = 26$ MHz, $f_{OUT} = 30 \dots 300$ kHz:
 - 1 Tone Generator A = 0.01 mm²
 - 2 Tone Generator A = 0.015 mm²

stop thinking
Never

Thank You for Your Attention!