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A Compact Multi-Tone Test Generator for RF ICs Using a ΣΔ - PLL

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***Abstract*—A new approach to adding built-in self test (BIST) capabilities to integrated RF transceiver chips is presented. An area efficient, all-digital building block generates multitone FM test signals in conjunction with a fractional-N phase locked loop without compromising the performance of the RF transceiver. The block itself is fully testable and consumes a chip area of only 0.015mm^2 in a 130nm CMOS technology. The spectral quality and reproducibility of the test signals are suitable for intermodulation distortion tests or PLL loop and jitter transfer measurements.**

I. INTRODUCTION

During the 1980's the increasing complexity of digital integrated circuits required new test concepts to improve testability and to bring down production test times. This led to the now well-known design-for-test (DfT) concepts like scan-chains, boundary scan and digital built-in self test (BIST) structures [1]. The 1990's brought the same paradigm shift to mixed-signal circuits. The main motivations for introducing Mixed Analog Digital BIST (MADBIST) concepts were the time consuming tests of high-resolution ADCs and DACs [1]–[4]. Now, integrated radio frequency (RF) circuits like wireless or high-speed serial transceivers have reached integration levels where again testability and production test time are becoming a bottle-neck. Special RF test equipment like spectrum analyzers and phase noise resp. jitter measurement units are expensive and signal frequencies in the GHz range are hard to handle in a noisy test environment.

The large statistical parameter spread and the low supply voltages of modern CMOS processes make the design of analog circuitry a challenging task; analog test circuitry creates additional failure modes which reduce the overall yield. On the other hand, the high integration density allows the realization of increasingly complex digital signal processing blocks with little area penalty. This makes a digital implementation of on-chip test circuitry an attractive option: it does not interfere with performance critical analog paths, it can be tested using well established digital test methodologies and its robustness causes little yield loss.

Multitone tests have long been used to characterize intermodulation distortions and frequency response of amplifiers, ADCs or RF modulators / demodulators: [2]–[4] present mixed A-D built-in self test (MADBIST) schemes consisting of digital biquad oscillators and a ΣΔ DAC for generation of multi-tone test signals to test both baseband ADCs and DACs. [5] extends this approach into the RF domain by using higher order images of the digital test signal to verify an RF receiver. Disadvantages of this method are that the amplitude of the higher order images is not very predictable and that two multiplexers need to be inserted into the critical RF path. [6] utilizes a digital sine generator to measure the jitter transfer function of a PLL, however his approach requires additional analog circuitry or an additional test clock at a multiple of the reference frequency.

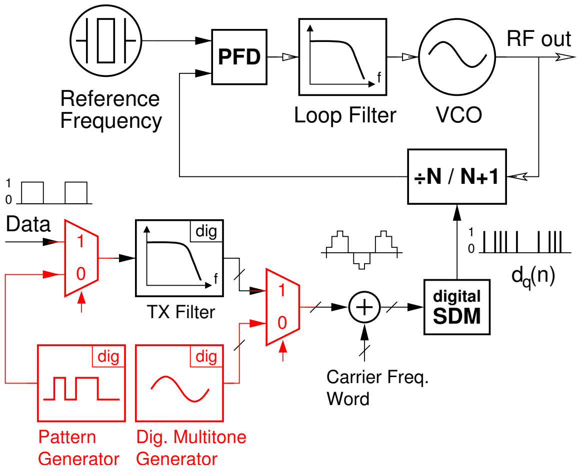

Fig. 1. Fractional-*N* modulator with added BIST blocks

This paper describes a concept which only modifies the

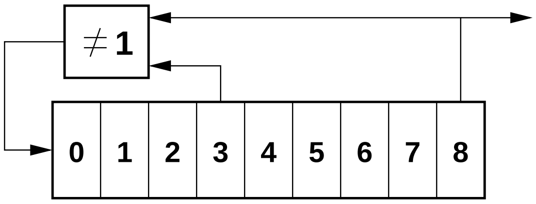

Fig. 2. Linear Feedback Shift Register (LFSR) with 9 bits

digital part and does not need additional clocks: A $\Sigma\Delta$ - Fractional-N Phase Locked Loop ($\Sigma\Delta$-PLL) can be viewed as a sort of DAC that converts digital data into phase instead of amplitude [7]. With this analogon in mind, some mixed-signal test concepts can be transferred into the phase / frequency domain of RF ICs. The fine frequency granularity of $\Sigma\Delta$-PLLs allows an indirect digital modulation of the VCO [8] by varying the PLL division ratio. This feature can also be exploited for test signal generation (fig. 1).

Generating a digital divider sequence does not interfere with the critical RF paths and allows generating nearly arbitrary test signals within the PLL loop bandwidth. One approach is to generate cyclic bit patterns like pseudo-random binary sequences (PRBS) or "01" sequences with a linear feedback shift register (LFSR) (fig. 2) and send them through the digital transmit filter ("Pattern Generator" in fig. 1). The additional test circuitry is very compact, consisting only of the LFSR and a MUX. However, the bandwidth of the test signals is limited to the bandwidth of the transmit filter, which usually makes it impossible to characterize the PLL near or above the loop bandwidth.

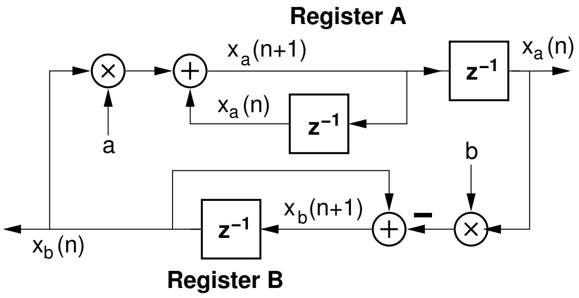

Fig. 3. Digital biquad oscillator

Another approach for creating test signals independently of the transmit filter is described in the next section:

II. PRINCIPLE OF DIGITAL SINE GENERATOR

The main building block for generating multi-tone signals in [2]–[5] is a digital biquad oscillator with quadrature outputs $x_a(n)$, $x_b(n)$ (fig. 3), realized with lossless digital integrators (LDI).

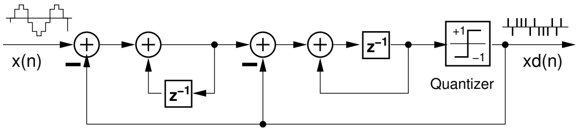

Fig. 4. Second order sigma-delta modulator

Relations for output signal frequency ω_{sig}, amplitude x_a, x_b and initial phase ϕ_a, ϕ_b of the biquad depending on sampling frequency f_s, coefficients a, b and the initial conditions $x_a(0), x_b(0)$ have been derived in [2]:

$$\omega_{sig} = f_s \cos^{-1}\left(1 - \frac{ab}{2}\right) \quad \text{for } 0 < ab \le 2 \tag{1}$$

$$\phi_a = \tan^{-1}\frac{\sin(\omega_{sig}T_s)\,x_a(0)}{(1-\cos(\omega_{sig}T_s)\,x_a(0) - ab) + a x_b(0)} \tag{2}$$

$$\hat{x}_a = \frac{(1-ab)\,x_a(0) + a x_b(0)}{\sin(\omega_{sig}T_s + \phi_a)} \tag{3}$$

Results for ϕ_b and $\hat{x}_b$ are attained by exchanging x_a with x_b and a with $-b$. For small coefficients $|ab| \ll 1$, the following approximations hold true:

$$1 - \cos\sqrt{ab} \approx \frac{ab}{2} \quad \text{and} \quad \cos^{-1}\left(1 - \frac{ab}{2}\right) \approx \sqrt{|ab|}$$

Using these approximations and setting $x_b(0) = 0$ gives the simplified relations

$$\omega_{sig} \approx \sqrt{ab}\, f_s \tag{4}$$

$$\phi_a \approx -\tan^{-1}\frac{2x_a(0)}{\sqrt{ab}} \approx \pi/2, \quad \phi_b = 0 \tag{5}$$

$$\hat{x}_a \approx \frac{x_a(0)}{\sin\phi_a} \approx x_a(0), \quad \hat{x}_b \approx x_a(0)\sqrt{\frac{b}{a}} \tag{6}$$

Eqn. (4) - (6) show that frequency and amplitude of the test tones can be set independently. The initial conditions can be optimized ($x_b(0) \neq 0$) for equal amplitudes x_a and x_b if good quadrature signals are required.

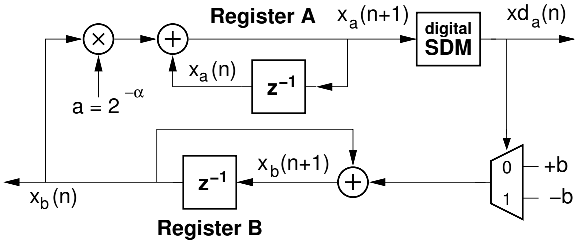

Fig. 5. Digital biquad oscillator using SDM attenuator

Directly implementing the circuit of fig. 3 in hardware requires two N x N bit multipliers. Another, more area efficient approach, is to replace one or both multipliers by a bit shifter, restricting the coefficient(s) to values of the form $2^{-\alpha}$. With two shifters only a very limited number of frequencies can be set, that's why a different approach was chosen.

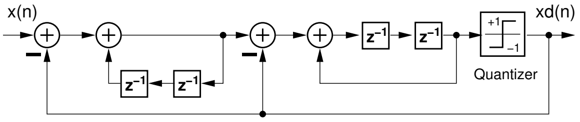

Fig. 6. Second order sigma-delta modulator for two time-multiplexed signals

One multiplier can be effectively replaced by a sigma-delta attenuator [3], [4]: A sigma-delta modulator (SDM) (fig. 4) converts an N-bit wide stream $x(n)$ into an oversampled single-bit stream $xd(n)$. Multiplying the single-bit stream with a constant b now only requires an N x 1 multiplier which is implemented as a multiplexer (fig. 5). In order to maintain the stability of the oscillator, an SDM like in fig. 4 with a latency of one sample clock has to be used.

Reconstruction of the original signal from an oversampled data stream only requires a low-pass filter which suppresses the higher order images of the signal created by sampling.

III. MULTI-TONE SIGNAL GENERATION

Multitone signals are generated by combining two or more sine generators. This can be performed by adding the signals from several sine generators, increasing the hardware complexity in a linear way with the number of required tones. A more economic approach is achieved by sharing the oscillator hardware using time division multiplexing [3]. All registers in the SDM (fig. 6) and the oscillator (fig. 7) are doubled up for each tone so that the tone signals are being processed independently. The adders and the bit shifter are shared among the signals which saves approx. 50% chip area compared to generating the tones individually.

Due to the time division multiplexing, the effective sampling frequency for L tones is reduced by a factor of L:

$$f_{s,eff} = f_s / L \tag{7}$$

This usually limits the useful number of tones, [3] gives a rule-of-thumb for the usable bandwidth of the oscillator of

$$f_{BW} \approx f_{s,eff}/150 \tag{8}$$

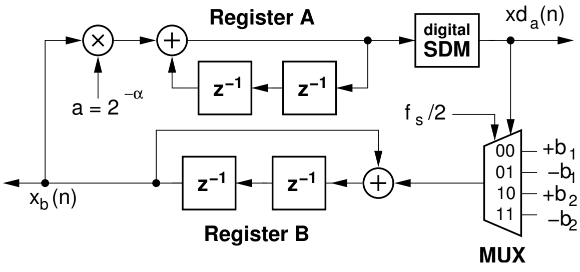

Fig. 7. Digital two-tone biquad oscillator using SDM attenuator

IV. RF SIGNAL GENERATION

The approach above can also be used for the generation of RF signals with multi-tone FM modulation when the DAC is replaced by a ΣΔ PLL. Multitone FM signals can e.g. be used to measure the frequency response of a PLL: the amplitude of a sideband within the passband is compared with another one outside the passband to check whether the closed loop bandwidth of the PLL is within the specified limits. Additionally, the multitone modulation can be used to test intermodulation distortion of the transmitter and receiver.

Due to the inherent low-pass characteristic of the PLL, no additional filter is needed to reconstruct the oversampled data stream of the test-generator.

The carrier frequency of a locked fractional-N PLL with integer division ratio N, fractional part $F = frac/2^{wf}$ and a reference frequency f_{ref} is given by

$$f_0 = f_{ref} \cdot N.F = f_{ref} \cdot \left(N + \frac{frac}{2^{wf}} \right) \tag{9}$$

where wf is the word length of the fractional accumulator. Frequency modulation is achieved by adding a modulation word $mword \cdot 2^g$ to the fractional word:

$$f_0(n) = f_{ref} \cdot \left(N + \frac{frac + mword(n) \cdot 2^g}{2^{wf}} \right) \tag{10}$$

Modulation with a digital sinewave with frequency f_{sig} and amplitude $\hat{m} = \max(mword) = 2^{w-1}$ produces a peak frequency deviation of

$$\Delta f_{max} = 2^g \cdot 2^{w-1} / 2^{bfrac} f_{ref} = 2^{g+w-1-wf} f_{ref} \tag{11}$$

corresponding to a maximum modulation index μ_{max} of

$$\mu_{max} = \Delta f / f_{sig} = 2^{g+w-1-wf} \frac{f_{ref}}{f_{sig}} \tag{12}$$

The resulting FM signal is

$$\begin{aligned} s_{FM}(t) &= A \cos\left(\omega_0 t + \mu \sin\left(\omega_1 t + \phi_1\right)\right) \\ &= A \sum_{n=-\infty}^{\infty} J_n(\mu) \cos\left(\omega_0 t + n\left(\omega_1 t + \phi_1\right)\right) \\ &\approx A \cos\left(\omega_0 t\right) + \frac{\mu A}{2} \cos\left(\omega_0 t \pm \omega_1 t\right) \qquad (13) \end{aligned}$$

For small modulation indices $\mu \ll 1$, the higher order Bessel terms decrease rapidly; the first terms can be approximated by: $J_0(\mu) \approx 1$, $J_{\pm 1}(\mu) \approx \pm \mu/2$.

Unfortunately, it is not possible to re-use the sigma-delta modulator of the PLL in fig. 1 as the SDM attenuator described above. The delta-sigma modulated stream of divide ratios not only contains the frequency modulation information but also the fractional frequency word. This constant offset needs to be eliminated from the SDM bit stream for proper operation of the biquad oscillator which is only practible for some special cases (0, 1/2, 1/4 etc.). Besides, the modulation gain 2^g would influence the signal frequency of the modulation sine wave and the modulation index at the same time which is undesireable.

The SNR of a signal which is quantized with k bits is

$$10\log SNR \approx 6k + 1.8\,\mathrm{dB} \qquad (14)$$

The above equation is only valid when the quantization error is uncorrelated. For a pure sine wave or multi-tone signal this assumption is not true and the spectrum will contain sidebands reducing the spurious free dynamic range (SFDR). Therefore, the needed word length to meet the spectral requirements is best determined by simulations. A SFDR of 60 dB was achieved by a word length of 15 bits.

V. RESULTS

Simulations were performed with a VHDL simulator, using the methodology described in [9]: The complete circuit in fig. 1 including the analog blocks like VCO and loop filter was modelled in VHDL, the period data of the VCO was dumped to a text file and post-processed using Matlab. Fig. 8 shows the simulated two-tone test signal at the output of a PLL with a loop bandwidth of 100 kHz, the x-axis being the offset frequency from the carrier. One tone is outside the loop bandwidth, it is attenuated by approx. 12 dB compared to the in-band tone. This ratio can be easily verified in a production test setup using a spectral analyzer. The spurious free dynamic range is nearly 60dB which is more than sufficient for frequency response measurements.

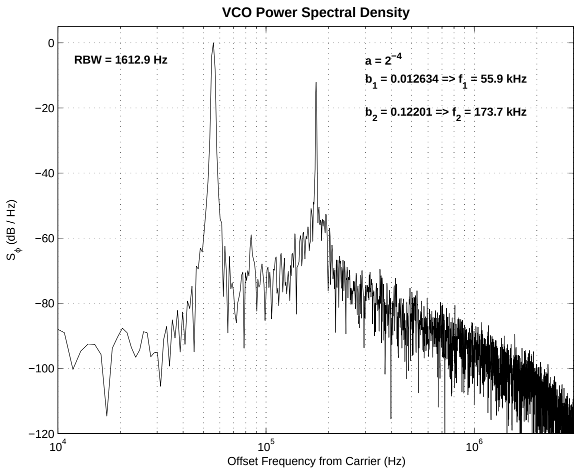

Fig. 8. Simulated two-tone spectrum at the PLL output

Two different programmable test tone generators have been synthesized and put on a test chip in a 130 nm CMOS technology. Table I shows the achieved frequency range and the chip area (excluding interconnect area).

Tones	Word Length	Min. Freq.	Max. Freq.	Area
1	15	31 kHz	365 kHz	0.01 mm^2
2	15	15 kHz	182 kHz	0.015 mm^2

TABLE I
IMPLEMENTED TEST-TONE GENERATORS

VI. CONCLUSION

An efficient method for generating PM / FM RF test signals on-chip has been presented that requires only little area overhead and does not interfere with critical RF signal paths as the signal generation is performed entirely in the digital domain. Possible test signals include PRBS or multitone PM/FM modulation allowing a fast verification of the entire transmit path.

VII. OUTLOOK

In order to reduce test costs even further, work is ongoing to analyze the PLL response on-chip as well. Such an architecture allows a complete Built-In Self Test (BIST), avoiding costly RF production test equipment. Built-In Self Calibration (BISC) strategies can also be implemented with this setup to increase the yield or to make the circuit more robust against environmental variations.

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