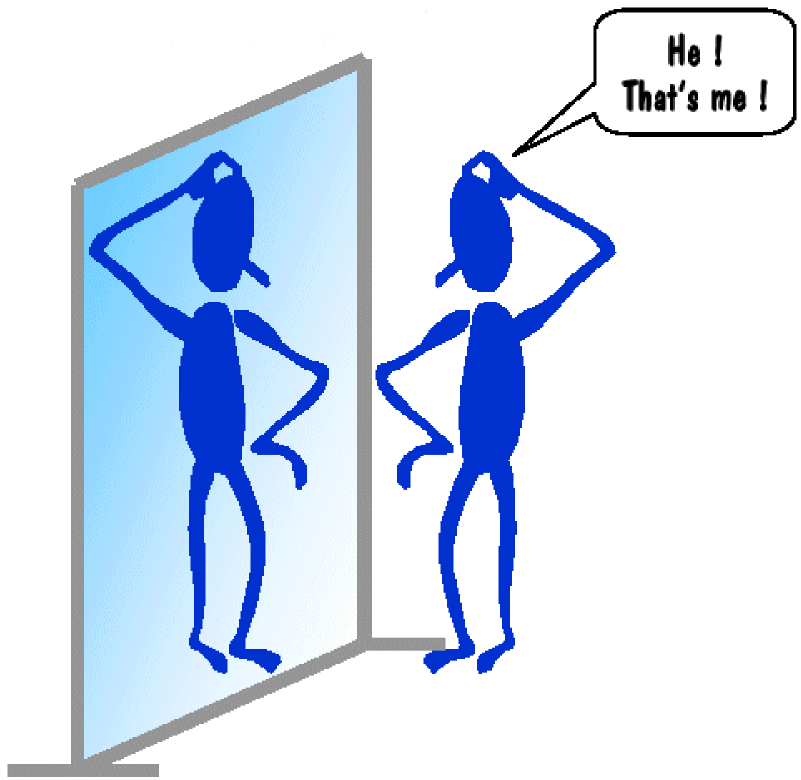
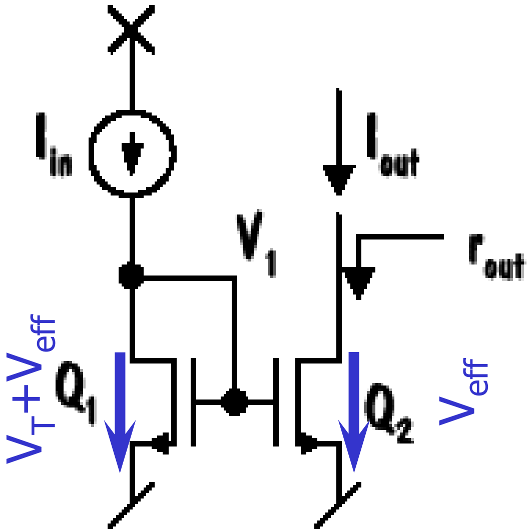
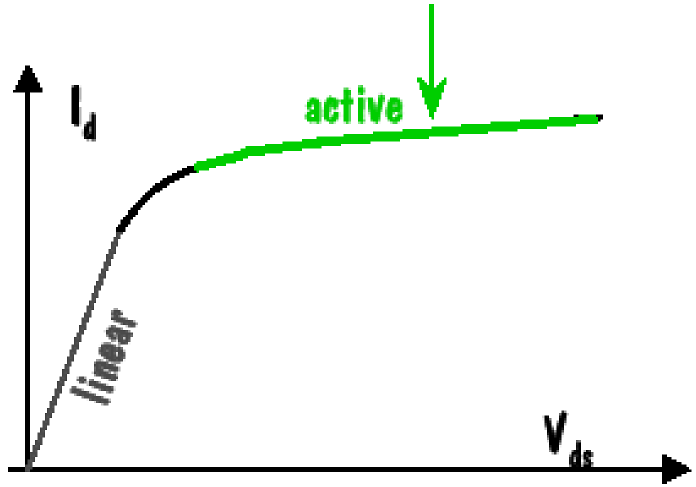
Current Mirrors Revisited



Basic Current Mirror



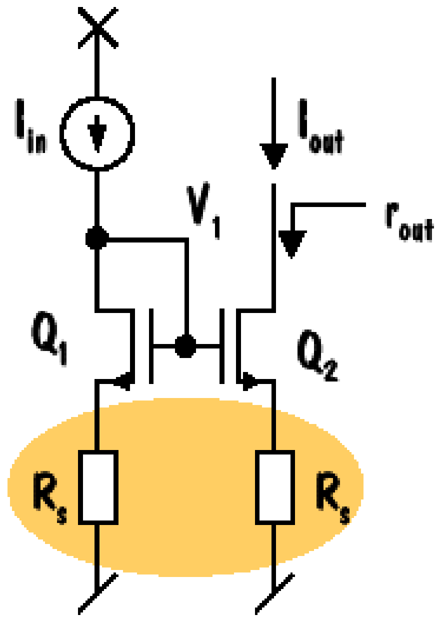


- fast and small
- high output voltage swing
- **but**: low output impedance $r_{out} \cong r_{ds2}$
  $\Rightarrow$ bad PSRR, high systematic error

Current Mirror With Source Degeneration

<u>Operation principle:</u>

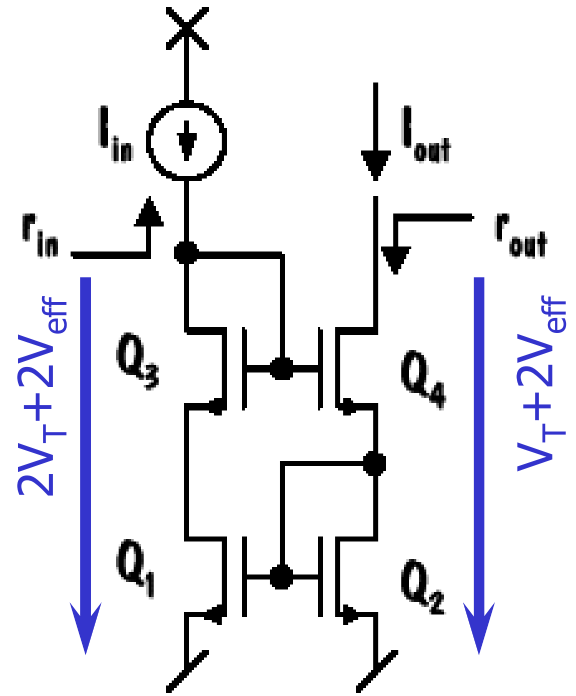
Negative feedback by R_S improves output impedance, 1/f noise and matching by $1 + R \cdot g_m \Rightarrow R \cdot g_m > 1$



- Needs same voltage drop on both sides
  $\Rightarrow W(Q_1) / W(Q_2) = R_{S2} / R_{S1}$
- Unefficient for low g_m devices (e.g. PMOS)
- Beware of resistor mismatch: additional mismatch term!

$$\sigma^2\left\langle \frac{\Delta R}{R} \right\rangle \cdot \left(\frac{Rg_m}{1 + Rg_m} \right)^2$$

Improved Wilson Current Mirror



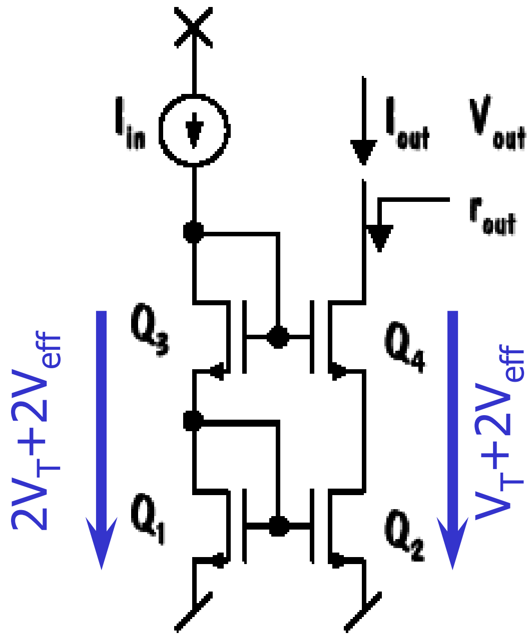
<u>Operation Principle:</u>
Q_2 senses output current, mirrors it to Q_1, V_{G4} changes if $I_{in} \neq I_{out}$ $\Rightarrow$ Feedback Loop!
Note: Q_3 helps to make $V_{DS2} = V_{DS1}$ („improved“)

- Similiar performance and headroom as stacked cascode
- Stability? Speed?

$\Rightarrow$ Advantages for bipolar technologies (compensation of base currents), but not recommended for CMOS

Stacked Cascode Current Mirror

<u>Operation principle:</u>
Cascode transistor Q_4 decouples V_{DS} of current source Q_2 from V_{out} and makes $V_{DS2} = V_{DS1}$, Q_3 provides bias voltage



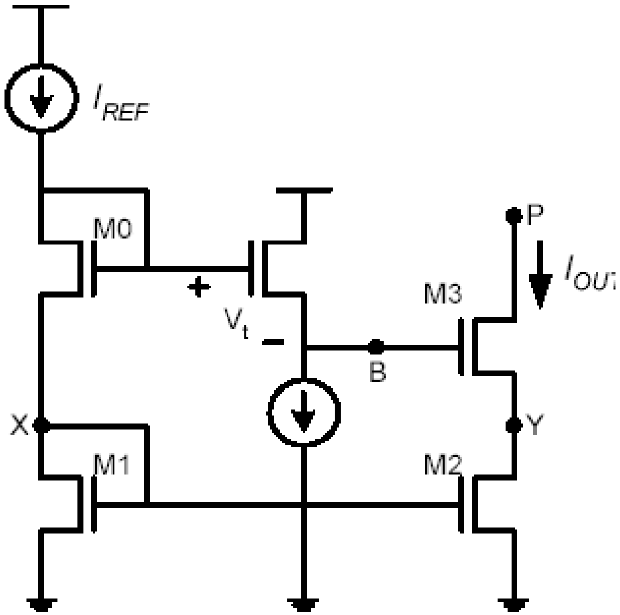
- Very high output impedance
  $r_{out} \cong r_{ds2} r_{ds4} g_{m4}$
- Big disadvantage is low input and output voltage headroom:
  $V_{out} > V_T + 2V_{eff}$
  $V_{in} = 2V_T + 2V_{eff}$

Cascodes: General Hints

- Make cascode devices as short as possible (headroom!)
- Increasing L increases output impedance somewhat
- For layout reasons, devices are usually made as wide as current source transistors
- Don‘t be afraid - cascode devices don‘t add noise or mismatch
- Use cascode devices for power down circuitry as well

Wide Swing Cascode Current Mirror (1)

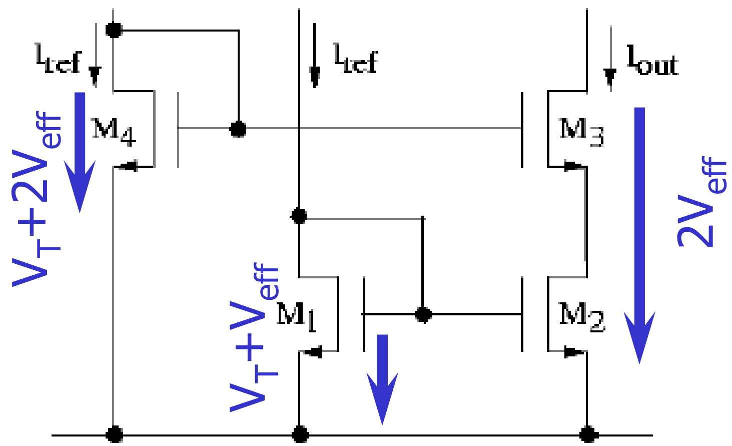
<u>Operation principle:</u>
Generate a lower bias voltage for cascode transistor M_3 by subtracting one V_T using a source follower



- Large output headroom $V_{out} > 2\ V_{eff}$
- Low input headroom: $V_{in} = 2V_T + 3V_{eff}$
- Difficult to dimension: M_3 and M_2 need to stay in saturation, $V_X = V_Y$ for good matching
  - $\Rightarrow$ not recommended due to lack of robustness!

Wide Swing Cascode Current Mirror (2)

<u>Operation principle:</u>
Generate a lower bias voltage for cascode transistor M_3 by using a second reference path with a smaller transistor

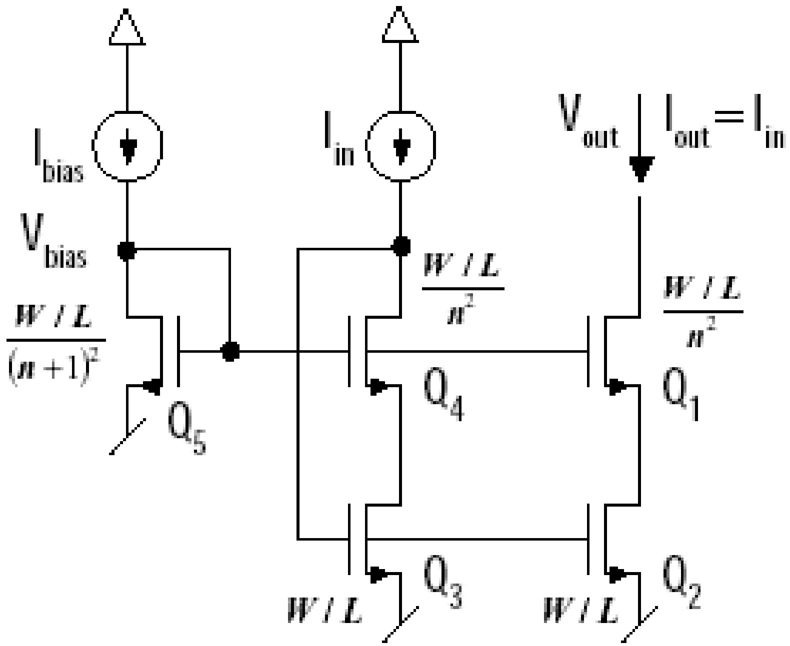


$$W_1/L_1 > 4 \cdot W_4/L_4$$

- Large output headroom $V_{out} > 2\ V_{eff}$
- Large input headroom:
  $$V_{in} = V_T + 2V_{eff}$$
- Systematic gain error: $V_{DS2} \neq V_{DS1}$!
  $\Rightarrow$ not recommended for high precision!

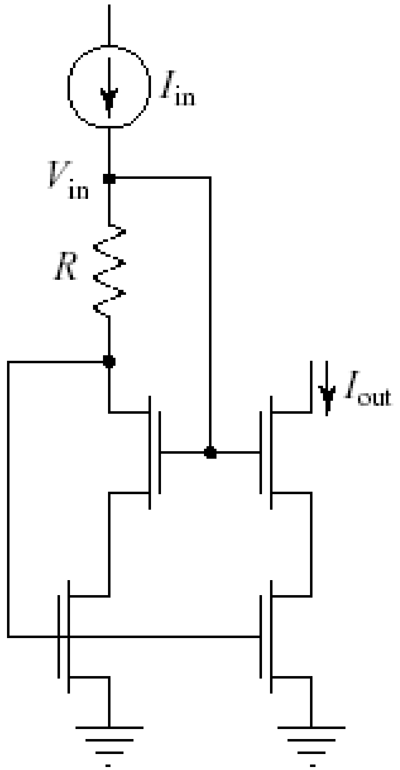
Wide Swing Cascode Current Mirror (3)

<u>Operation principle:</u>
The gate potential of Q_3 rises until Q_3 can sink I_{in}. Size Q_1 and Q_4 such that Q_2 and Q_3 are not driven into triode region



- Large output headroom: $V_{out} > 2\ V_{eff}$
- Large input headroom: $V_{in} = V_T + V_{eff}$
- Precise current ratio: $V_{DS2} = V_{DS1}$
- Robust: even works in triode region $\Rightarrow$ recommended for high precision and low voltages

Don‘t ...



Brooks & Rybicki

- Saves one bias current path compared to last design BUT ...
- Sensitive to technology/temperature variations, voltage drop across R must be big enough to keep devices in saturation
- At least, do extensive simulations!

Do's and Dont's (Design)

- Check for sufficient headroom at low supply voltages, high temperatures and increased input current
- Scale resistors / switch transistors in the source path with the transistor width
- Use wide swing cascodes instead of stacked ones
- Carefully check power-down modes for floating nodes and HCS conditions

Do‘s and Dont‘s (Layout)

- Use unity size elements with same orientation (matching!)
- Use shadow devices (matching!)
- Use common-centroid layout (matching!)
- Use star connection for source currents (voltage drop)
- Don‘t route Metal1 across the mirror (matching, stress)
  - if necessary, route across all devices identically
- Don‘t place mirrors near large poly areas, N-Wells or STI (matching, stress)
- Make current mirrors metal-programmable, add spare devices if area allows