A Quad-Band Low Power Single Chip Direct Conversion CMOS Transceiver with ΣΔ-Modulation Loop for GSM

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Outline

• Overview
  – C11 120 nm CMOS Technology
  – Transceiver Architecture

• Block Detail
  – Voltage Controlled Oscillator
  – $\Sigma\Delta$-Phase Locked Loop
  – Power Amplifier

• Performance Summary
C11 120nm CMOS Technology

- 120 nm RF Transistor with $f_T > 100$ GHz ($V_{DD}=1.5V$)
- Oxide thickness 2.8 nm
- 400 nm analogue I/O Transistor ($V_{DD}=2.5V$)
- 6 Copper layers up to 550 nm thick
- MIM CAP (1 fF/um$^2$)
- Diffusion and Polysilicon Resistors
GSM Transceiver Features

- Direct Conversion RX and TX
- Supported Bands 850/900/1800/1900 MHz
- Internal RX and TX VCO
- $\Sigma\Delta$-Modulation Loop for GMSK
- Constant gain receiver for 14 bit ADC
- Part of complete GSM/GPRS Platform
- 48-pin VQFN Plastic Package
VCO with digital bias and band select

- Pushing < 300 kHz/V
- Integrated low noise voltage regulator
- Programmable frequency band (10 bit)
- Programmable bias current
Voltage Controlled Oscillator Core

- Differential Cross Coupled
- MOS Tuning Element
- VCO gain 60 MHz +/-10%
- 1300 MHz frequency range
10 Bit VCO: Frequenz vs. Binärwort

Frequency Accuracy: 2 MHz per bit
Delta-Sigma Frac.-N PLL Modulation Loop

\[ \text{fref} = 26 \text{ MHz} \]

20 bit accuwidth in MASH
⇒ high loopfilter suppression needed at 400 kHz, but the modulation needs to have a wide bandwidth!
Concept of Predistortion Filter

\[
\frac{\Phi_{\text{out}}(s)}{\Phi_{\text{ref}}(s)} = N \cdot \frac{1}{1 + \frac{N}{K_P K_{\text{VCO}}} \frac{1}{sZ(s)}} = N \cdot G(s)
\]

\[
f_{\text{out}}(s) = N_{\text{mod}}(s) \cdot f_{\text{ref}} \cdot G(s) \cdot G(s)^{-1} = N_{\text{mod}}(s) \cdot f_{\text{ref}}
\]
Power Amplifier

- Differential Output
  - 1.5 V Supply Voltage
  - Drives 50 Ohm Load
  - Broadband (flat over band)
  - Low Noise

- Separate 900/1800 MHz Outputs
  - 8.5 dBm @ 900 MHz
  - 8 dBm @ 1800 MHz
High margin to GSM Specification due to low phase noise
PLL Settling Time

analog PLL settling time < 80 µs
Chip Photograph
## Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>GSM850/GSM900</th>
<th>GSM1800/1900</th>
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<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>57 dB</td>
<td>57 dB</td>
</tr>
<tr>
<td><strong>Noise Figure</strong></td>
<td>2.6 dB</td>
<td>3 dB</td>
</tr>
<tr>
<td><strong>1 dB Compression</strong></td>
<td>-22 dBm</td>
<td>-22 dBm</td>
</tr>
<tr>
<td><strong>IIP2</strong></td>
<td>50 dBm</td>
<td>50 dBm</td>
</tr>
<tr>
<td><strong>RX Phase Noise</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>@ 600 kHz</td>
<td>-129 dBc/Hz</td>
<td>-123 dBc/Hz</td>
</tr>
<tr>
<td><strong>TX Phase Noise</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>@ 40 kHz</td>
<td>-96 dBc/Hz</td>
<td>-100 dBc/Hz</td>
</tr>
<tr>
<td>@ 20 MHz</td>
<td>&lt;-162 dBc/Hz</td>
<td>&lt;-157 dBc/Hz</td>
</tr>
<tr>
<td><strong>Phase error</strong></td>
<td>1.4 °</td>
<td>1.6 °</td>
</tr>
<tr>
<td><strong>TX Output Power</strong></td>
<td>8.5 dBm</td>
<td>8 dBm</td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TX</td>
<td>210 mW</td>
<td></td>
</tr>
<tr>
<td>RX</td>
<td>250 mW</td>
<td></td>
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</tbody>
</table>
Conclusion

• Fully integrated GSM CMOS Transceiver
• New TX-architecture with ΣΔ-Modulation Loop
• New constant gain receiver concept
• Complies with GSM Specification