



processor available. Since a conventional PGC is omitted in a constant gain receiver there is no further need for a higher order channel preselect filter and a DC-offset correction. Both are required for linear operation of the PGC especially under GSM interference conditions. To counteract gain deviations caused by process and temperature variations mainly in the RF devices (including frontend losses) of the receive path a programmable gain correction stage is added to ensure always accurate adaptation to the input dynamic range of the ADC. Additional coarse gain steps cover the compatibility to various baseband ICs. The required ADC resolution is mainly determined by the GSM reference sensitivity and reference interference level specifications. A 30 dB gain step ensures the receiver's functionality for higher wanted signal levels up to -15 dBm at the antenna. Fig. 2 shows the baseband signal level vs. antenna input level in a constant gain receiver.

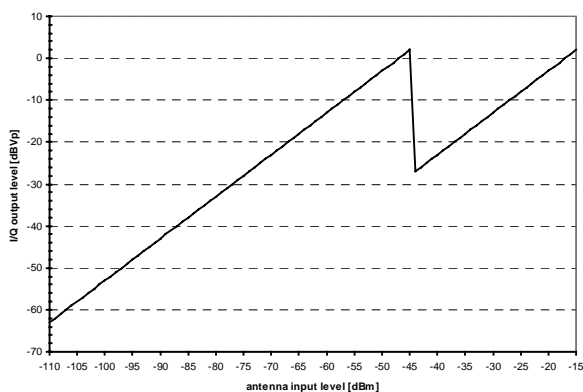


Figure 2 GSM constant gain receiver principle

Each of the four bands is using a differential, inductively degenerated LNA with resistive load and an ingeniously realized gain step. To meet all system requirements (noise figure, linearity, harmonic suppression and CMRR) careful balancing of the design is necessary, especially finding the optimum trade off between wideband matching network and noise performance. A standard Gilbert cell for downconversion was chosen to achieve low LO leakage into the RF path. The resistive load of the Gilbert cell combined with an external capacitor forms a passive pole ensuring linearity under GSM blocking conditions. To prevent an exceeding influence of flicker noise to the overall noise performance the switching mixer transistors are driven by a LO-signal with high slew rate generated by several inverter structures. To assure high IIP2 an accurate symmetrical layout is inevitable. A multiple feedback biquad in combination with the passive pole at the mixer output forms a 3rd order baseband filter which provides sufficient selectivity to avoid an ADC overdrive at the corresponding GSM reference interference levels. The biquads impedance level is a trade off between noise performance and chip area. A programmable gain correction stage with 1 dB steps over a wide range tops the design.

#### 4. VCO

A single fully integrated VCO is running at 3.8 GHz, twice the frequency of the highest GSM1900 band to minimize interaction with the received and transmitted signals. With this architecture, the frequency range of approximately 1300 MHz including sufficient margin for temperature, process and supply voltage tolerances can be addressed. Prior to the receive or transmit process, coarse tuning of the VCO frequency is achieved by switching capacitors to the LC tank, chosen by a digital 10 bit control word, setting the divided frequency with an accuracy of better than 2 MHz. The VCO core comprises a cross coupled NMOS pair with an integrated coil for the LC tank, NMOS varactors for analog tuning and a coil for additional noise filtering [2]. All active elements are thin oxide devices with gate lengths chosen larger than the minimum length in order to decrease the 1/f noise corner frequency. The VCO core current is supplied by a PMOS current source. Biasing circuitry and VCO core are both supplied by an on-chip voltage regulator providing an output voltage of 2.1 V. The VCO amplitude is controlled by variation of the core current depending on the selected frequency band, in order to achieve constant VCO gain ( $K_{vco}$ ) and to protect the active devices in the core, while maintaining a high oscillation amplitude for low phase noise. Due to the accurate digital tuning to the required frequency, analogue fine tuning can be restricted to the range of a few MHz, therefore the  $K_{vco}$  can be kept at a low value of 60 MHz/V with a small tuning voltage range of less than 200 mV.

Crucial for the operation of the system is a frequency respectively phase of the VCO that is independent of supply variations. Capacitive coupling of the varactors to the VCO core reduces the sensitivity of the VCO to supply variations and together with the low  $K_{vco}$  and usage of the integrated voltage regulator, a pushing figure of < 300 kHz/V is realized.

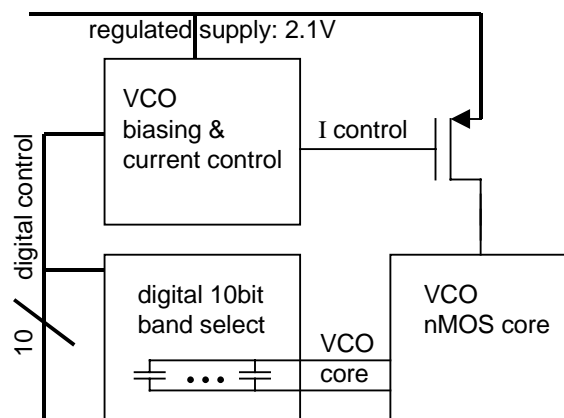


Figure 3 Block diagram of VCO with digital control of biasing and band select.

## 5. Modulation Loop

The proposed modulator architecture depicted in Fig. 4 uses the technique of predistortion where the bandwidth of the signal exceeds the closed loop bandwidth of the synthesizer. This technique allows direct modulation of the VCO within the closed loop, without restriction due to the loop bandwidth of the fractional-N frequency synthesizer.

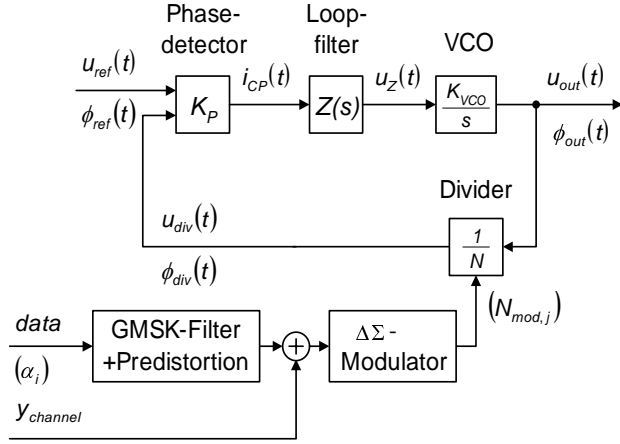


Figure 4 Fractional-N modulator using predistortion

This is possible because of a digital compensation respectively predistortion filter with a transfer characteristic equal to the inverse of the closed-loop transfer function  $G(s)$ . A similar technique is presented in [3]. The transfer function derived from Fig. 4 is given by

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = N \cdot \frac{1}{1 + \frac{N}{K_p K_{VCO}} \frac{s}{Z(s)}} = N \cdot G(s) \quad (1)$$

where  $N$  is the divider value,  $K_p$  [A/rad] and  $K_{VCO}$  [rad/Vs] are the conversion gain values for the phase-detector and the VCO respectively.  $Z(s)$  [ $\Omega$ ] is the Laplace transformation of the loop filter transimpedance.

If the output frequency of the VCO  $f_{out}(s)$  of the fractional-N frequency synthesizer is modelled as presented in [4] the transfer characteristic for  $(N_{mod,j})$  is given by

$$f_{out}(s) = N_{mod}(s) \cdot f_{ref} \cdot G(s) \quad (2)$$

whereas  $N_{mod}(s)$  is the according representation in the complex variable domain. When the modulation data is filtered by the inverse of the closed-loop transfer function  $G(s)$  the output frequency of the VCO can be derived as

$$f_{out}(s) = N_{mod}(s) \cdot f_{ref} \cdot G(s) \cdot G(s)^{-1} = N_{mod}(s) \cdot f_{ref} \quad (3)$$

Because the loop transfer function is very sensitive to

parameter variations a constant open loop gain is achieved by a digital adjustment algorithm OLGA<sup>2</sup> (Open Loop Gain Auto Adjustment). This algorithm performs measurements of the open loop gain at VCO-frequency and controls the current of the charge-pump to ensure a constant open loop gain.

Core element of this new modulation loop architecture is a novel fractional-N frequency synthesizer. The value of the synthesized frequency is determined by the division factor of a new low power multi-modulus divider. This divider covers a divider range from 16 up to 255 by increments of 1 and results in a modulation of the VCO at VCO-frequency. To control the divider values in the feedback path of the fractional-N frequency synthesizer a third order multi stage noise shaping (MASH) architecture with 23 bit wide accumulators is used to reach the desired noise shaping performance. Due to a utilized reference frequency of 26 MHz at the input of the modulation loop a frequency resolution of 3 Hz at VCO-frequency is achieved. The digital input data to the MASH-modulator is the sum of the desired channel-frequency and the modulation data filtered by a Gaussian filter as defined by the GSM standard and the appropriate predistortion filter. The well known problem of linearity that is required from the phase-detector can be solved by using a non-integrating loop filter with flat group delay in combination with pulse width modulation at the output of the phase-detector.

The TX buffer amplifies the output signal of the divider to drive a programmable maximum power level of 8 dBm into an external differential 50  $\Omega$  load. The combined noise level of VCO sideband noise and the noise floor of divider and buffers are better than -162 dBc at 20 MHz frequency offset in the GSM900 band. No external SAW and 3<sup>rd</sup> harmonic filters are needed to fulfil the GSM specification of transmitter noise emitted into the receive band [5].

## 6. Realization

The transceiver has been designed in standard 120 nm CMOS technology with six copper metalization layers. The gate oxide thickness is 2.8 nm. Metal-Insulator-Metal capacitances (MIM) of 1 fF/ $\mu\text{m}^2$  density with low coupling into the substrate are used for the RF-circuits. The drain source voltage of the MOS transistors with 120 nm gate length can be stressed up to 1.5 V. Analogue I/O transistors of 400 nm minimum gate length with 2.5 V breakdown voltage are used for the design of bandgaps and operational amplifier. The package of the chip is a VQFN48 housing. The chip photograph is shown in Fig. 5.

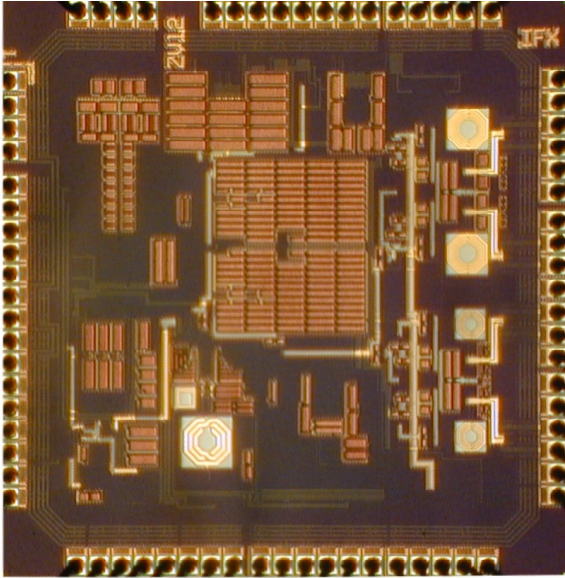


Figure 5 Chip micrograph

## 7. Measurement Results

Due to the low phase noise of the synthesizer a phase error of  $1.6^\circ_{rms}$  is achieved over all conditions. The output spectrum of the transmitter in the 900 MHz band is shown in Fig. 6. The GSM specification for the modulation mask can be fulfilled with 8 dB margin as shown in Fig. 7. A PLL lock-in time of  $70 \mu s$  has been measured including the time needed for the VCO alignment and is depicted in Fig. 8.

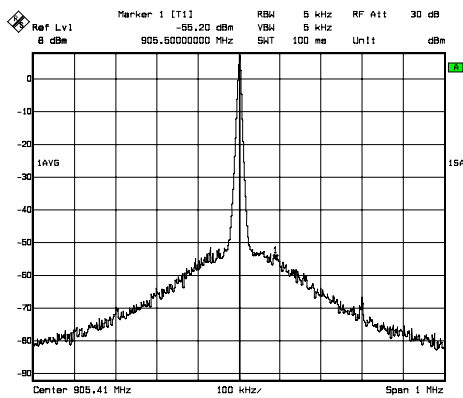


Figure 6 Output Spectrum

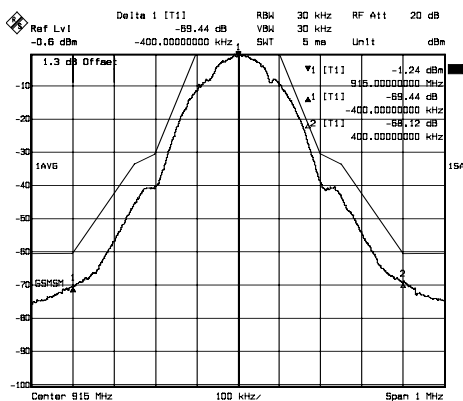


Figure 7 Modulation Spectrum

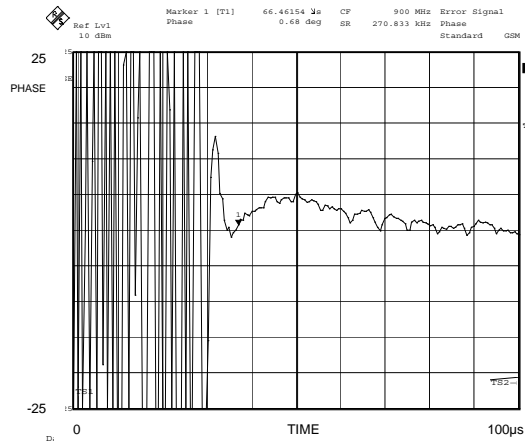


Figure 8 PLL lock-in time

	GSM850/GSM900	GSM1800/1900
Gain	57 dB	57 dB
Noise Figure	2.6 dB	3 dB
1 dB Compression	-22 dBm	-22 dBm
IIP2	50 dBm	50 dBm
RX Phase Noise @ 600 kHz	-129 dBc/Hz	-123 dBc/Hz
TX Phase Noise @ 40 kHz	-96 dBc/Hz	-100 dBc/Hz
TX Phase Noise @ 20 MHz	< -162 dBc/Hz	< -157 dBc/Hz
Phase error	1.4°	1.6°
TX Output Power	8.5 dBm	8 dBm
Power consumption		
TX	210 mW	
RX	250 mW	

Figure 9 Performance Summary

## 8. Conclusion

A fully integrated quad band transceiver chip in standard CMOS technology including a new  $\Sigma\Delta$  modulation loop architecture with digital predistortion has been presented. An automatic loop gain adjustment and a VCO with digital pre-tuning has been implemented. The GSM specifications are fulfilled with a phase error below  $1.6^\circ$  over all bands. A signal to noise ratio of  $-162 \text{ dBc}$  at 20 MHz offset to the carrier has been reached without needing a SAW filter in the TX path. The very simple constant gain direct conversion RX architecture offers low noise performance and small chip size but is demanding for 14bit ADC resolution at the baseband processor. The power consumption is only 210 mW in transmit mode and 250 mW for the receiver.

## References

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